

**GCE**

**Electronics**

Unit **F614**: Electronic Control Systems

Advanced GCE

**Mark Scheme for June 2015**

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All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

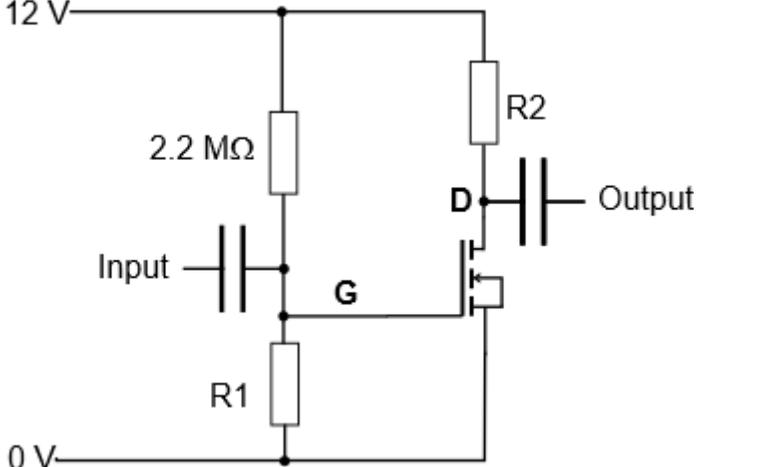
Mark schemes should be read in conjunction with the published question papers and the report on the examination.

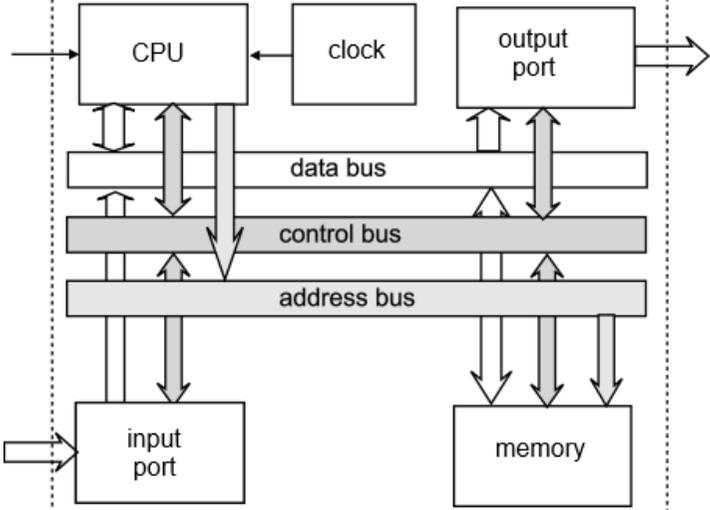
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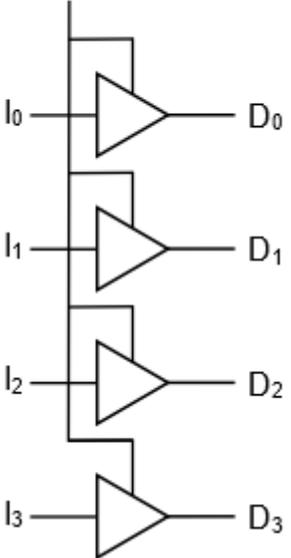
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## Annotations

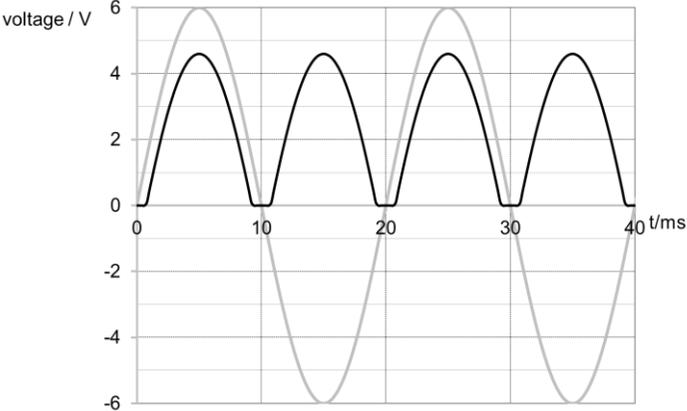
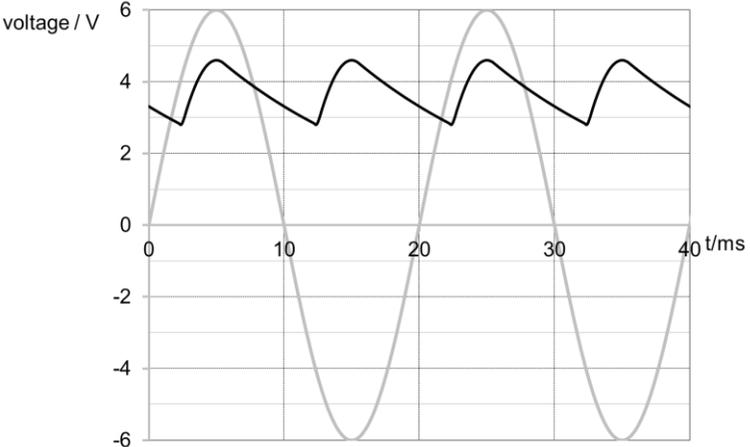
Annotation	Meaning of annotation
	Blank Page – this annotation <b>must</b> be used on all blank pages within an answer booklet (structured or unstructured) and on each page of an additional object where there is no candidate response.

Question	Expected answer	Mark	Additional guidance
1a	Input to G output from D Connections through capacitors	1 1 1	 <p>12 V</p> <p>2.2 MΩ</p> <p>Input</p> <p>R1</p> <p>G</p> <p>R2</p> <p>D</p> <p>Output</p> <p>0 V</p>
1b	Voltage across 2.2 MΩ = 12 – 2.7 = 9.3 V Current through 2.2 MΩ = 9.3 / 2.2 × 10 <sup>6</sup> = 4.22 × 10 <sup>-6</sup> R1 = 2.7 / 4.22 × 10 <sup>-6</sup> = 639 kΩ	1 1 1	Any answer which rounds to 640 kΩ
1c	80 mS = 0.08 S	1	77 mS – 83 mS
1di	So that the voltage at D can wobble up and down (wtte) By a large amplitude (wtte)	1 1	Reference to ac Or negative comment about avoiding saturation
1dii	pd across resistor = 12 – 7 = 5 V R2 = (12 - 7) / 0.04 = 125 Ω (ecf voltage)	1 1	
1e	G = -g <sub>m</sub> × R <sub>DS</sub> = - 0.08 × 125 = -10 Values from 1c and 1dii multiplied (ecf) Minus sign	1 1	

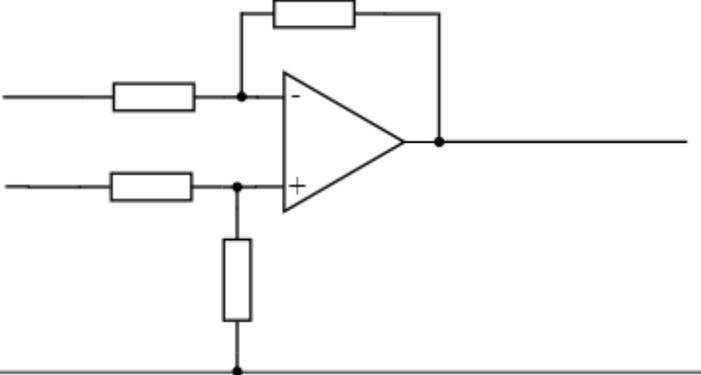
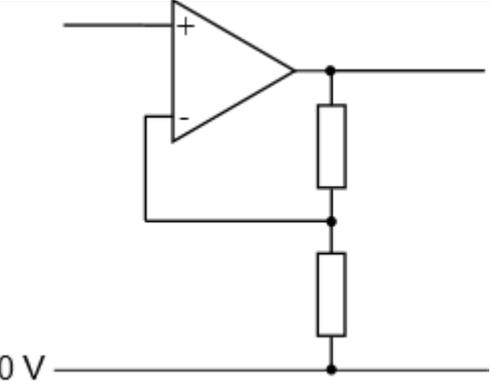
Question	Expected answer	Mark	Additional guidance
2a	1 mark for each correct label	5	 <p>The diagram illustrates a computer system architecture. At the top left is a box labeled 'CPU'. To its right is a box labeled 'clock' with an arrow pointing to the CPU. Further right is a box labeled 'output port' with an arrow pointing to the right. Below these are three horizontal bars representing buses: 'data bus', 'control bus', and 'address bus'. At the bottom left is a box labeled 'input port' with an arrow pointing to the left. At the bottom right is a box labeled 'memory'. Bidirectional arrows connect the CPU to each of the three buses. The data bus also has bidirectional arrows connecting it to the output port and the input port. The control bus has bidirectional arrows connecting it to the output port and the input port. The address bus has bidirectional arrows connecting it to the output port and the input port. The memory is connected to the data bus, control bus, and address bus with bidirectional arrows. The entire system is enclosed in a dashed-line box.</p>
2b	collection of wires carrying data <u>to and from/bi-directional</u> between CPU (clearly CPU in all circumstances) and memory/input/ouput port	1 1 1 1	

Question	Expected answer	Mark	Additional guidance
2c	4 tri-states Common enable connected to read Outputs connected to D <sub>0-3</sub> Inputs connected to I <sub>0-3</sub>	1 1 1 1	read 
2d	Maximum 2 from: Storing programme Storing look up table Storing data from input port Storing data from calculations	2	
2ei	In CPU	1	
2eii	Register Containing the <u>address</u> Of the next instruction	1 1 1	Allow memory in CPU (wtte)

Question	Expected answer	Mark	Additional guidance
3a	$2^n$ Evidence of using 7 address lines	1 1	$2^7 = 128$ [2]
3b	$128 \text{ (ecf)} \times 6 = 768$	1	
3c	$2^5 - 1 = 31$	1	
3d	Disables chip (wtte) One from: <ul style="list-style-type: none"> <li>• Preventing read or write function (wtte)</li> <li>• High impedance state on data lines (wtte)</li> <li>• So that other memory modules can access the data bus</li> </ul>	1 1	
3e	Values all 0 V or 5 V $A_5 = 5 \text{ V}, A_4 = 5 \text{ V}, A_3 = 5 \text{ V}, A_2 = 0 \text{ V}, A_1 = 5 \text{ V}, A_0 = 0 \text{ V}$ $\overline{\text{CE}} = 0\text{V}$ $\overline{\text{Read}} = 0\text{V}$ $\overline{\text{Write}} = 5\text{V}$	1 1 1 1 1	ecf 1 instead of 5  ecf 1 instead of 5

Question	Expected answer	Mark	Additional guidance
4a	Output all positive Full wave rectification Max voltage 4.6 V (by eye) 0 V flat around zero crossing	1 1 1 1	
4b	Capacitor in parallel with resistor	1	
4c	Max voltage 4.6 V (ecf) Output wobbles all > 0 V Correct (asymmetric ripple) shape voltage drop to approx. half max voltage [allow min between 2 V and 3 V] Period = 10 ms 14 ms	1 1 1 1 1 1	

Question	Expected answer	Mark	Additional guidance
4d	Max 2 from: Smoother output Fixed voltage More efficient Lighter/smaller	2	
4e	Oscillator produces high freq ac for transformer Transformer changes <u>large</u> ac voltage to <u>small</u> ac voltage Rectifier turns ac to dc Smoother keeps voltage above zero all the time Comparator compares output with constant voltage from reference Opto-isolator turns on oscillator when output too low	1 1 1 1 1 1 1	Allow current change

Question	Expected answer	Mark	Additional guidance
5a	The camera would keep moving and never settle (hunting) So the picture would not be stable	1  1	
5b	Correct circuit Circuit with negative feedback All resistors 1 kΩ or more Both input resistors the same and both other the resistors the same	2 1 1 1	
5c	Working amplifier circuit For non-inverting amplifier With gain of +2 Power supply labelled (0 V)	1 1 1 1	

Question	Expected answer	Mark	Additional guidance
5d	P eventually settles at 5 V and then -10 V Evidence of slowing as P approaches R E starts at 5 V E = R - P (by eye) D = 2 x E E and D saturate at -13 V at transition of R	1 1 1 1 1 1	



Question	Expected answer	Mark	Additional guidance
7a	$(5 \times 33000) / (22000 + 33000) = 3 \text{ V}$	1	Or by ratios
7b	$2 / 6 \times 10^{-3} = 333 \ \Omega$	1	Or other values from graph giving $R_{DS} = 300 \ \Omega - 350 \ \Omega$
7c	$V \text{ across MOSFET} = 5 - 3.4 = 1.6$ $I = 1.6 / 333 = 4.8 \text{ mA (ecf)}$	1 1	
7d	Similar shaped curve with shallower gradient below existing curve (transistion not beyond existing curve transistion) Max 2 from: $I_{DS}$ reduced $R_{DS}$ increased Less current through LED (so dimmer)	1 2	
	Total	107	
	QWC	3	Overleaf
		= 110	

**Quality of Written Communication**

- 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
- 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
- 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
- 0 The language has no rewardable features.

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