GCE

Electronics

Advanced GCE **A2 H465**

Advanced Subsidiary GCE **AS H065**

OCR Report to Centres June 2016

OCR (Oxford Cambridge and RSA) is a leading UK awarding body, providing a wide range of qualifications to meet the needs of candidates of all ages and abilities. OCR qualifications include AS/A Levels, Diplomas, GCSEs, Cambridge Nationals, Cambridge Technicals, Functional Skills, Key Skills, Entry Level qualifications, NVQs and vocational qualifications in areas such as IT, business, languages, teaching/training, administration and secretarial skills.

It is also responsible for developing new specifications to meet national requirements and the needs of students and teachers. OCR is a not-for-profit organisation; any surplus made is invested back into the establishment to help towards the development of qualifications and support, which keep pace with the changing needs of today's society.

This report on the examination provides information on the performance of candidates which it is hoped will be useful to teachers in their preparation of candidates for future examinations. It is intended to be constructive and informative and to promote better understanding of the specification content, of the operation of the scheme of assessment and of the application of assessment criteria.

Reports should be read in conjunction with the published question papers and mark schemes for the examination.

OCR will not enter into any discussion or correspondence in connection with this report.

CONTENTS

Advanced GCE Electronics (H465)

Advanced Subsidiary GCE Electronics (H065)

OCR REPORT TO CENTRES

F611 Simple Systems

General Comments

Analysis of marks awarded show most candidates had a good understanding of the aspect of electronics being examined with very few candidates omitting questions, indicating that most candidates have acquired a good grounding in electronics across the whole specification. In general, candidates find written answers more challenging than calculations although some of the answers to numerical questions by weaker candidates indicate misconceptions about basic electricity. The best candidates show an excellent grasp of the subject with some clear and concise explanations and a range of good solutions to questions. This report will highlight the areas where candidates did not do so well in order to aid teachers and students in preparation for future exams.

Comments on Individual Questions:

Question 1 provided a relatively straightforward start to the paper. About one in five candidates had problems with the Boolean expression for the EOR gate. The most challenging part of the question was the explanation with little evidence of candidates using the truth table to produce a relatively straightforward answer leading to some contradictory, unclear or incomplete answers.

Question 2 started with a common calculation which most candidates can perform but there remains a significant proportion of candidates who do not calculate the PD across the resistor by using ideas of voltages in series circuits indicating some basic misconceptions.

The graph in 2b was completed accurately by just over half the candidates, a surprising number failed to use the information in the question to ensure that their line went through 2.2 V, 15 mA, other errors included the transition to conduction at 0.7 V, the current saturating at 15 mA for large voltages and showing a negative breakdown voltage.

Question 2c discriminated well with a good spread of marks, a number of candidates thought that the LED was in reverse bias.

The graphs in 2e were generally of a good standard, the main issues were with the poor exponential decay curves for **A** and some behaviour at 35 s which looked like recalling the sudden step down in voltage at the end of the period for a two NAND gate monostable circuit rather than continuing the decay to 50 s.

Question 3 proved a generally challenging question. Correctly drawing the MOSFET symbol continues to be an issue for many candidates, a high proportion of the answers to part (a) featured incorrect MOSFET symbols. There were a significant number of candidates who did not connect the MOSFET in series with the speaker and seemed uncertain about what to do with the connections from the loudspeaker.

Question 3e was the least well answered question on the paper. Some candidates got muddled and wrote ‘when it is hot’ twice. Many thought that the loudspeaker would sound at hot temperatures and really didn’t understand the oscillator and when it would function. A common misconception was that a speaker operates like a buzzer and makes sound when a dc voltage is present across its terminals. Many candidates did not appreciate the function of the diode in the circuit and incorrectly assumed that when the output of the temperature sensor was 5 V the voltage at **F** was 5 V. Instead of writing about voltages as directed, many candidates wrote about the points being high or low and so missed the subtleties of the circuit.

Question 4. The marks for question 4 were generally good with the majority of candidates getting 3 or 4 marks, part e providing the most challenge.

Question 5 discriminated well. The answers to 5a often lacked detail and clarity with very few candidates obtaining full marks. Parts b to e presented few problems for most candidates but many found 5f difficult often missing the 2.7 V. Many candidates did not appreciate that the bulb will light regardless of polarity and there were a number of comments about the diode protecting the bulb. A number of students forgot to subtract the voltage across the diode when calculating power in 5h but 5i was usually fine.

Question 6 proved straightforward for most candidates with a number simplifying the expression before drawing the circuit, whilst this was not necessary it produced a smaller circuit.

Question 7. The main issues in question 7 were drawing the diagram in 7b with few problems in the calculation but R and C often interchanged or the 0 V connection omitted.

Question 8 produced lots of good marks at the end of the paper showing that candidates had sufficient time. In 8a a number of candidates forgot the bar for **F**. The truth table was generally correct. Some candidates failed to mark the letters in 8c which does not allow examiners to see if part of the circuit is correct so marks can be lost. 8d produced a range of correct answers although some answers were too brief to gain the mark.

F612 Signal Processors

General Comments

The paper produced a wide range of scores, broadly consistent with those of recent years. A relatively small number of excellent scripts were seen whilst, at the other extreme, candidates scored very weakly, often displaying lack of preparation. Of these, a small number expressed frustration through comments which, albeit inoffensive to the examiner, bore no relation to the material of the questions and were sometimes critical of candidates' preparation by Centres. The large majority of attempts at all questions, up to and including 8(c), gave evidence of adequate time to complete the examination.

Good understanding of most of the included circuits was reflected in responses. Completeness, rather than correctness, was lacking to various degrees in many descriptive responses and was a significant factor in marks being forfeited.

Subsequent to the printing of the question paper, an inconsistency was identified in Question 6(b). Here the timing of the reset pulse after 7 intervals of P and A, being incompatible with the initial count of 001 shown on the timing diagram, means that the diagram could not be completed satisfactorily. Consequently, in fairness to all candidates and in consultation with the subject manager, the decision was taken to award the full score of 4/4 to all candidates, thereby removing any discrimination of 6b from the overall assessment.

Comments on Individual Questions:

Question 1

a) Candidates showed good understanding of the sequential behaviour of flip-flops, most appreciating the need for alternate operation of switches M and L to activate/deactivate the LED.

b) Correct feedback connections were added to most diagrams, the main loss of marks being reversal of the S and R inputs.

Question 2

a) Was correct on a large majority of scripts, with only a single Input and Output labelled. Almost all showed correct synchronous clocking.

b) Most candidates understood the need for successive falling and rising 'Clock' edges to transfer a data bit completely from Input to Output. Many marks were lost, however, through ambiguous references to labels 'D' and 'Q' and not specifying to which flip-flop these referred, or by failure to mention that each is 'frozen' then 'transparent' alternately.

Question 3

Most parts of this question scored well, except (c) where many answers failed either to specify +/-13V saturation levels or to provide evidence of a supporting calculation to justify the maximum input value given in the question. Incorrect calculation of the Gain in (b) inhibited scoring this second mark.
Although a relatively small number omitted part (d) completely, component values calculated from appropriate formulae usually led to good scores. Ironically perhaps, the main loss of marks was through incorrect circuit diagrams.

Question 4

(a) Was very well answered, almost all candidates obtaining the correct numerical result.

(b) The truth-table was completed correctly on the majority of scripts.

(c) Also had high facility, even though several candidates provided no response.

(d) Linking appropriate Boolean expressions to all of X, Y and Z in (b) proved too challenging for many candidates, although most correctly linked at least X, and sometimes Y. Incorrect responses in (b) could not generally invoke 'error carried forward', as such answers could very rarely be matched to any of the expressions supplied.

Question 5

(a) Provided the lowest facility of any part-question on the entire paper. Very few answers made any reference to Gain, most being incorrect or incomplete assertions that Output is inversely related to 'Resistance'. There was very little evidence of understanding Potential Divider function. The 3rd mark required only a simple appreciation of the capacitor's role in impeding low frequency signals or blocking D.C., but a significant number of candidates made no reference to it. Those who did generally earned this mark.

(b) Summing-amplifier circuits were frequently incorrect, common mistakes being non-inverting amplifiers, amplifiers with only a single input, and inputs tied to supply rails. Where possible, the mark for correct resistor values was awarded but, although the correct formula was commonly quoted, responses did not go on to apply it convincingly.

(c)(i) Was well-answered, many earning full credit. Base-Cut 'Bode' plots and linear, or inconsistent logarithmic, frequency scales, although quite rare, were the most common reasons for loss of marks. Break Frequency calculations were very well done and 'roll-off' usually correctly drawn.

(ii) Scored quite poorly, through failure to emphasize that it is high frequencies which are suppressed and following this with suitable examples.

(d)(i) The need for current amplification was generally appreciated, low current output of the preceding stages being the more commonly cited alternative to earn the 2nd mark.

(ii) Almost all stated the correct numerical value of 0V. Thereafter, with decreasing frequency, came V+ = V-, use of negative feedback and (in extremely few cases) high open-loop gain. As a consequence, the maximum mark was hardly ever scored.

Question 6

(a) In line with most questions requiring descriptive answers, the main loss of marks was through incompleteness rather than lack of understanding. Many answers gained only the first mark, despite the mark scheme providing 4 alternatives to earn the other 2. Very few referred to the' logic' or 'driver' functions of circuit X. Others were too vague on explaining the creation of codes to show decimal numbers on the 7-segment display.

(b) As explained above, answers to this part-question were not included for assessment.

(c) Again, incompleteness of answers incurred penalties to varying degrees for all but a small minority. Explicit links between flip-flop reset and suppression of pulse generation at P, and 'NOT Q' becoming logic 1 providing the impulse for counter reset, were required independently, but rarely seen. Also, candidates did not emphasize that the display would show the sequence 1, 2, 3 before resetting. Many wasted time and space on repeated descriptions of the decoder function, already covered in (a).

Question 7

(a) (i) Was poorly answered, with many answers linking output of each preceding stage to input of the following thereby resulting in a circuit similar to that of Q2a.

(ii) As for Q6a, the 3 marks could be scored via a range of opportunities, of which full advantage was not always made. Answers stating, or implying, that registers can themselves perform calculations/comparisons were not credited, nor were answers merely citing storage of digital 'words' rather than the more explicit examples required.

(b) Was a high-facility question, answered correctly by most.

Question 8

(a) In (i), a frequent mistake was 'let So = 00' (rather than 80 as required). This had some repercussions for b (ii), but ECF was applied sympathetically there.

(b)

(ii) Was correctly answered in most cases, but some candidates wrongly assumed that logic 0/1 at any given output pin automatically resulted in non-activation/activation of the connected component. Again, ECF was applied wherever appropriate in b (ii).

(c) (i) Was correct on the majority of scripts.

(ii) Scores suffered again through incompleteness of explanations, in particular explicit reference to 'c' as the point to which the program reverts until S4 has been decremented to 00, and that the relevant outputs flash on and off 3 times.

(d) Testing the input for '40', followed by a direct link to 'e', was correct in most cases. Incorrect steps in programming and/or syntax mistakes were quite widespread.

F613 Build and Investigate Electronic Circuits

General Comments

The vast majority of centres have developed a good understanding of both the coursework process and the correct administration procedure for the submission of marks and the sending of report samples to moderators. For those new to the process or as a reminder to more experienced practitioners, the following comments have been made by moderators which merit inclusion in this report.

A small number of centres did not send the moderator the MS1 form. This form is needed to check entries and is a vital part of the coursework package. Centres have the option of completing the traditional carbon copy MS1 with its 3 identical sheets; one sent to OCR so that marks can be entered on the system, one for the centre to keep as a record, and one to be sent to the moderator. Some centres use OCR's Interchange system where marks can be inputted online by the centre. A copy of the MS1 is available using this system and it is the Exam Officer who usually has access to this. Whichever system is used, the moderator must receive the MS1.

It was encouraging to see more centres making good use of annotated comments on the scripts. This indicates regions of a report where marks have been awarded. The majority of centres are correctly highlighting these areas but some centres are still highlighting areas of a report with an inappropriate criterion.

Most centres have a library of tried and tested circuits to be investigated at this level. With these, candidates have a number of different circuits to investigate and it can be arranged so that candidates do not do the exact same circuit. Even for the same circuit theme, for example, a voltage amplifier, with different component values, every candidate can investigate a unique circuit. A small number of centres have submitted work where all the candidates have attempted the exact same circuit which I do not think is appropriate and I encourage these centres to revisit their circuits and introduce some diversity to the circuits given for investigation.

In terms of the raw marking, most centres achieved a good level of appreciation of the mark scheme and its application. Moderators largely agree with the raw marks and most centres are within tolerance. For some centres, a small number of marking criteria are a problem: Criterion 1a is important as it sets out the circuit under investigation, how the circuit works, its predicted behaviour and thus, what is to be tested. An appropriate use of the circuit must be given for the full mark of 4/4 to be awarded. Some suggested uses were not deemed appropriate. For example, for a relaxation oscillator it would not be appropriate to suggest that a 'clock' is a suitable use. One has to be more specific to be awarded this mark for a suitable use. Also for 1a, to be awarded 4/4 the circuit must be described at a qualitative level. A few candidates did not do this but had been awarded full marks for this section.

- Test plans (1b) are sometimes a problem. Far too many candidates are using the past tense to describe their testing. They start by saying, 'This is what I did to test the subsystem…..' (or some similar expression). This approach is not a plan but a history of the testing done. This does not gain any marks. A test plan should be an organised and detailed 'wish list' of how the testing is to be done and with what equipment. How the equipment is to be used is also important. There should be consideration of:
    - How the subsystem is to be fully tested
    - With what equipment
    - How that equipment is to be used
- For the circuit photograph of the build quality (2a), the photograph must be in colour to enable colour coding of the circuit to be moderated. Too many photographs were in black and white.

- Test results (3b) must be presented in table or data form.
- Analysis of test results (3c) must be thorough and relate back to circuit predictions.
- For diagrams (4a), test diagrams must show the positioning of test equipment using the correct circuit symbol and be correctly placed.

I would like to take this opportunity to thank everyone involved with this process. A tremendous amount of work goes into the setting of the work, the marking of the work, the preparation for the submission of marks and the sending of the samples. I fully appreciate the time and effort that is involved.

F614 Electronic Control Systems

General Comments

Candidates showed evidence of a good understanding of the aspect of electronics being examined with very few candidates omitting questions. Many candidates find written answers more challenging than calculations. The best candidates show an excellent grasp of the subject with some clear explanations and a range of imaginative solutions to questions. This report will highlight the areas were candidates did not do so well to aid teachers and students to prepare for future exams.

Comments on Individual Questions:

Question 1

1 a and b were a relatively straightforward start for most candidates with many candidates solving part a by ratios and inputting through a capacitor to X although there were other correct solutions.

Some candidates lost marks in 1c(i) because the line at 3.3V was drawn sloppily and missed the correct point, the diagonal line would have benefitted from the use of a ruler in many of these cases.

In 1d(i) the input signal was sometimes considered and not the ac output, the weaker answers indicated a lack of understanding of this part of the circuit.

The weaker candidates did not grasp the Kirchoff's rules which led to lost marks in 1d(ii) with the correct voltage often missed with 5V or 9V used instead of 4V. This issue is also prevalent in AS papers.

Again, careless construction in 1e gave unclear answers and lost marks with the gradient line very wobbly. A significant few thought the line had the same gradient as the V_{GS}= 5V line.

Question 2

The action of the thermistor and its role in determining voltage at T was often missed in 2b.

The graphs in 2d were generally good; the main problem here was the voltage at D was often put as starting high

In 2e most candidates mentioned that proportional control gave less/no hunting but few could say why. On/off control was answered better but a few could not clearly give the reason why it was quicker to respond than proportional feedback.

Question 3

Answers to 3a showed that many candidates did not appreciate that this was an example of on-off feedback with the role of the oscillator poorly understood. Many gave the impression that the oscillator was always on but when the output voltage dropped the oscillator increased its frequency.

Many answer to 3b put the rectification as full wave. Some put it as half wave but with a voltage drop of 1.4V.

3cii proved challenging, many candidates missed the correct ratio here. Using constant current to solve the problem was not often used.

Question 4

Many candidates found 4b difficult with 0 V incorrectly given as the answer for ii.

4c was answered well but 4d proved more challenging with a good range of marks. Most candidates scored well but few got full marks.

Question 5

5a and 5b were mostly well answered but a significant number of candidates failed to give 7E as the number to output in 5a.

Some of the poorer answers in 5c missed the point about explaining the use of registers and instead tried to describe the code in quite general terms without specifically focusing in on registers.

5d was a challenging question with many possible correct solutions. Whilst there were some excellent answers to this, many candidates lost marks by outputting 01 to activate the dp losing the number on the seven segment display. A significant number of candidates had difficulties with the delays; the line 'wait200ms' with nothing else was often seen with no associated code to implement this subroutine.

Question 6

6a and b were mostly answered well but some missed that the output was the inverse of X.

6c was also well answered by most; the most challenging aspect seemed to be drawing a common data line by connecting the output of the read tristate to the input of the write tristate.

Question 7

This final question proved generally challenging with all candidates able to write something but many not being able to explain themselves well enough to get full marks.

In 7a candidates were often vague about the function of general purpose registers – some candidates added all they knew about registers to the question.

7b was generally poorly answered with few candidates saying anything worthwhile about the pivotal position of the CPU with the data bus. A minority of candidates seem confused about the nature of the data bus, confusing it with a register or memory location for storing data.

7c proved challenging for many candidates. Some described a machine cycle, many failed to alter the stack pointer. A substantial number of candidates failed to distinguish well between the stack pointer and the stack.

Despite all of the issues highlighted, the scripts were of a generally good standard with some examples of excellent and innovative solutions to problems by candidates that had clearly received a good practical education in electronics.

F615 Communication Systems

General Comments:

The paper appears to have challenged the most able whilst allowing all candidates to obtain some credit. There were a few unused marks at each end of the scale, with some bias towards the higher marks, perhaps to be expected as candidates should have had prior experience of AS work. Candidates seemed on the whole to be well prepared, though there were occasional scripts where the candidates did not offer enough to do themselves justice.

There were some common issues, such as getting the order of LSB and MSB reversed when dealing with counters, forgetting to put in units in answers, not indicating the 0 Volt rail in diagrams, incorrectly converting between scientific notation and standard prefixes.
Some candidates who were capable of scoring well on questions which needed calculations, or the recall of circuits, did less well when faced with the need to 'explain' i.e. to put their ideas into words. Some took invalid routes, others missed out significant points, limiting their score.

Comments on Individual Questions:

Question 1 This turned out to be quite a challenge for two reasons:
1a some candidates did not appreciate that the count had to reach 4 for the line sync pulse to be triggered, and those who did often reverse the MSB and LSB on the counter

1b More candidates realised that the line count had to reach 100, but the MSB /LSB confusion again occurred.

Many did not make it clear that the frame and line sync signals are pulses, and referred to them rather vaguely.

1ci Some good answers, though often the bandwidth was not converted to a bit rate. Many correctly commented on the flicker or lack of it, in line with their calculations.
1cii Often well answered, though some assumed that reducing the bandwidth would reduce the refresh rate.
1d The calculations were usually well done, though one, and sometimes both, of the input and output NOT gates were frequently omitted, and some candidates displayed forgetfulness of the layout of a NAND gate monostable. The typical error was to exchange resistor and capacitor.

Question 2
2ai Reading the needed information from the graph challenged many
2aii The pattern of side-bands and carrier was often correctly represented, despite the side-band spacing having been wrongly calculated in the previous section.
2b Generally well done

Question 3
3ai Calculation usually well done
3aii Sometimes candidates did not make it clear that they were referring to radio waves
3bi OK
3bii Often calculated their own way, but with the correct result
3biii OK

Question 4
4ai Usually well done
4aii Usually well done, the main problem was the phase relationship between the square wave and the direction of ramping of the triangle wave.
4aiii Usually correct, sometimes by alternative method of calculation.
4b Nyquist was often invoked in explaining why the sampling frequency had to be 2x the highest signal frequency.
4c Clearly well taught, often all correct

Question 5
5a Sometimes candidates were let down by the lack of clarity in their explanation.
5b The attenuation of the signal was often not referred to
5c Usually well done

Question 6
6a Often all correct
6bi Often all correct, common errors were not recalling the unit of inductance, not converting correctly to standard prefixes.
6bii A challenge to produce a clear explanation, which was met by some

Question 7
7a Often all correct
7bi+ii Often all correct
7biii ECF was allowed only for a complete reversal of the Truth Table
7c Some completed the question, though the Summing amplifier formula was infrequently seen as such, many gave equivalent calculations. It was common to reverse the values of R_a and R_b, so that R_a was half R_b

Question 8
8a Often all correct
8biii Clarity of expression was key to scoring well on this question
8biii Partial credit was available for incorrect calculation of the range or the number of steps

Question 9
9a Good candidates made it clear that one, and only one, of the signals, S_0 -S_3, appeared at the output L, depending on the value of the binary word BA – one word, one signal.
9b Some candidates did not make it clear that the signals were present on the link for a **short** time, **one after another**.

F616 Design Build and Investigate Electronic Circuits

General Comments:

The 2016 examination series has demonstrated that some centres have shown an excellent understanding and application of the marking criteria whilst some centres are over-generous with the raw marking of certain criteria. With only a maximum number of 60 marks available for the report, it is quite easy to fall outside of tolerance. Effectively, if only two or three criteria have been marked too generously this can push the raw mark outside of tolerance. Thus, the importance of understanding the criteria and being consistent in its application are vital.

It was good to see that more centres have used meaningful annotations in the reports. These not only aid the marking process but also make the moderation process easier. The annotations only need to be very brief and show where a mark has been awarded. The use of annotations can focus the marker on where marks have been achieved in the report; this can form the basis of an effective, accurate marking system.

Another trend that moderators have commented on is that a small number of centres have submitted reports on projects which are extremely similar in nature. I believe that it is good practice for all candidates in a given group to attempt projects which are sufficiently unique. It is the responsibility of the centre to ensure that, as far as possible, this uniqueness is maintained. It should be quite easy to ensure that candidates do not attempt to do the same project.

In terms of the raw marking and the problems encountered, moderators report that it is the same criteria that continue to cause problems. For this reason, these criteria are discussed below:

- **Research** (1a) continues to cause trouble for some centres. In order to award the higher marks candidates must put in writing the research that has been carried out; used referenced evidence of relevant sources of research. Ideally, there should be some useful data obtained from the research.

- **The specification** (1b) not only applies to the full circuit but also to each subsystem. It is the combination of both which leads to the final mark for 1b. Power supplies are an obvious specification point missed out by many.

- **Test plans** (1c) cause problems even though it is an integral part of the AS course. If a candidate states how a test was done this will score zero marks. The plan should be a discussion of how a particular subsystem is to be tested, with what equipment, and how; clearly described how testing was to be performed. Diagrams should also be included showing the position of test equipment. Do not forget that the final circuit also needs a test plan.

- **The description of circuits** (2b) were poor. In order to achieve the higher marks, systems must be described from a component view; described in detail the circuit behaviour.

- **Fault-finding** (2e) must be explicit in the report ; shown evidence of a thorough testing programme on the final circuit and all subsystems.

- **The displaying of results** (3b) must use either tables or graphs; presented the results of the tests in an appropriate manner. When tables are used for digital results moderators want to see actual voltage levels and not digital levels 1/0.

- **Results analysis** (3c) is a difficult criterion to achieve high marks as it involves high level skills candidates need to show that they have; analysed the test results and achieved the specification . Too many candidates are awarded high marks for this criterion with no justification and it is the most common criterion that moderators disagree with the raw mark. Specification points must be considered in the analysis and so must the testing of the final circuit and how that compares to the specification. It has been noticed that few candidates test the final circuit with a thorough test routine which also compromises the mark for criterion 3d.

- **Diagrams** (4a) must be correct to score marks and must show all component values.

Should any centre feel that further clarification or support is needed with this module then please contact OCR http://www.ocr.org.uk/.

Finally, I would like to thank everyone who has been involved with the successful completion of this module.

OCR (Oxford Cambridge and RSA Examinations)
1 Hills Road
Cambridge
CB1 2EU

OCR Customer Contact Centre

Education and Learning
Telephone: 01223 553998
Facsimile: 01223 552627
Email: general.qualifications@ocr.org.uk

www.ocr.org.uk

For staff training purposes and as part of our quality assurance programme your call may be recorded or monitored

Oxford Cambridge and RSA Examinations
is a Company Limited by Guarantee
Registered in England
Registered Office; 1 Hills Road, Cambridge, CB1 2EU
Registered Company Number: 3484466
OCR is an exempt Charity

OCR (Oxford Cambridge and RSA Examinations)
Head office
Telephone: 01223 552552
Facsimile: 01223 552553