OCR
Oxford Cambridge and RSA

Wednesday 13 January 2016 – Afternoon

LEVEL 1/2 CAMBRIDGE NATIONAL IN SYSTEMS CONTROL IN ENGINEERING

R113/01 Electronic principles

Candidates answer on the Question Paper.

OCR supplied materials:
None

Other materials required:
- A calculator may be used

Duration: 1 hour

Candidate forename		Candidate surname	

Centre number						Candidate number				

INSTRUCTIONS TO CANDIDATES

- Use black ink. HB pencil may be used for graphs and diagrams only.
- Complete the boxes above with your name, centre number and candidate number.
- Answer **all** the questions.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).
- Do **not** write in the bar codes.

INFORMATION FOR CANDIDATES

- The total number of marks for this paper is **60**.
- The number of marks for each question is given in brackets **[ ]** at the end of the question or part question.
- Dimensions are in millimetres unless stated otherwise.
- Your quality of written communication will be assessed in questions marked with an asterisk(*).
- This document consists of **12** pages. Any blank pages are indicated.

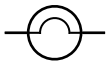
Answer **all** questions.

1 **(a)** Complete the table by naming the unit for each quantity shown.

Quantity	Unit
Capacitance	
Frequency	

[2]

(b) Name the two component symbols shown in Fig. 1.



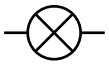


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Fig. 1

[2]

(c) A resistor has a current flowing through it of 10 A and a voltage across it of 220 V.

Calculate:

(i) the value of the resistor in ohms

.....

..... **[2]**

(ii) the power, in watts, absorbed by the resistor.

.....

..... **[2]**

(d) Determine the total resistance of a circuit made up of two resistors in series of value 18 Ω and 22 Ω.

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..... **[2]**

2 Fig. 2 shows a D type bistable with a positive edge trigger.

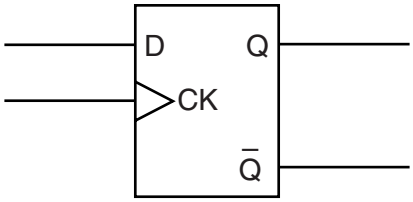

Fig. 2

(a) State the meaning of each of the connections.

Terminal D .....

.....

Terminal CK .....

.....

Terminal Q .....

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Terminal $\overline{Q}$ .....

.....

[4]

(b) Complete the timing diagrams for a positive edge-triggered D type bistable shown in Fig. 3.

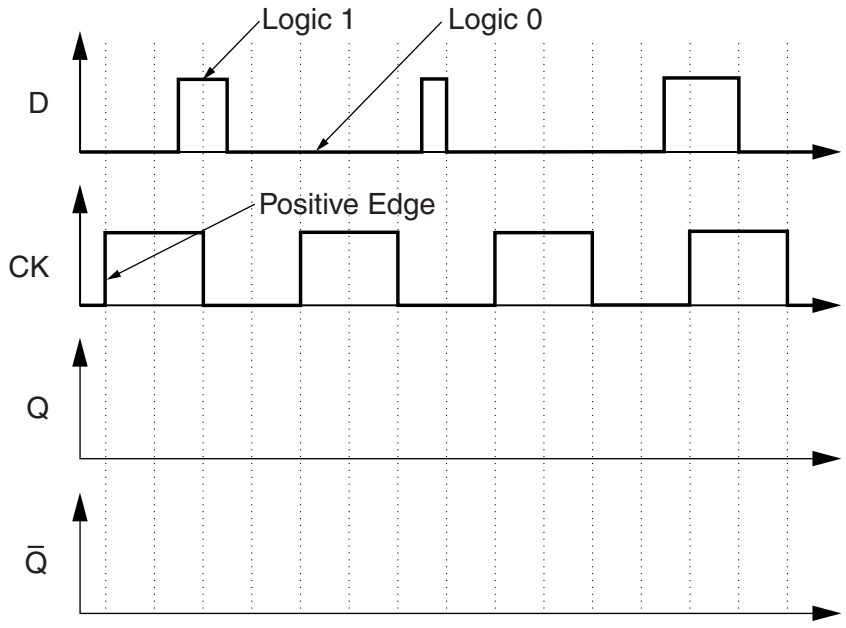


Fig. 3

[2]

(c) For a different situation, complete the timing diagrams for a positive edge-triggered D type bistable shown in Fig. 4.

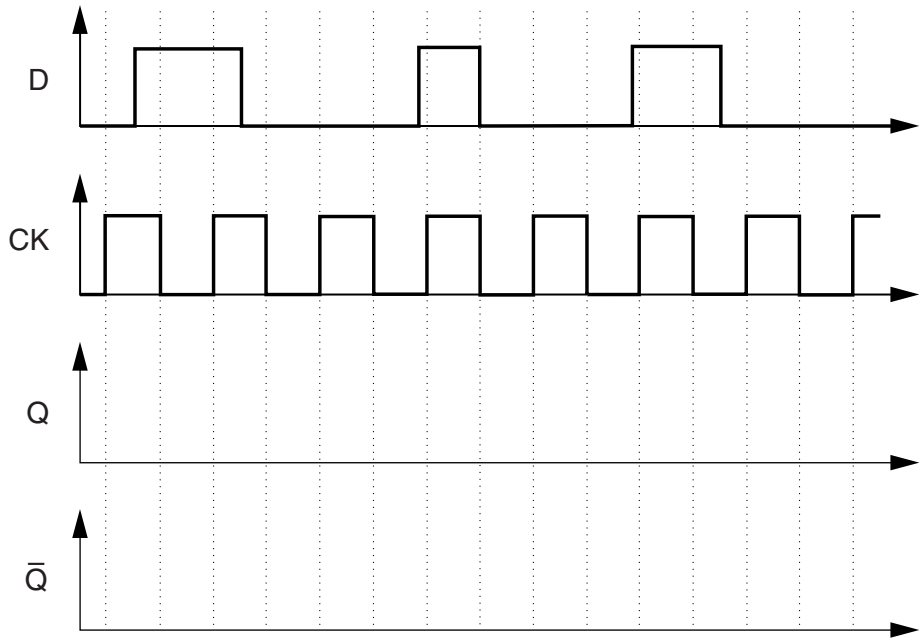


Fig. 4

[4]

3 Fig. 5 shows part of a potential divider circuit using an NTC thermistor.

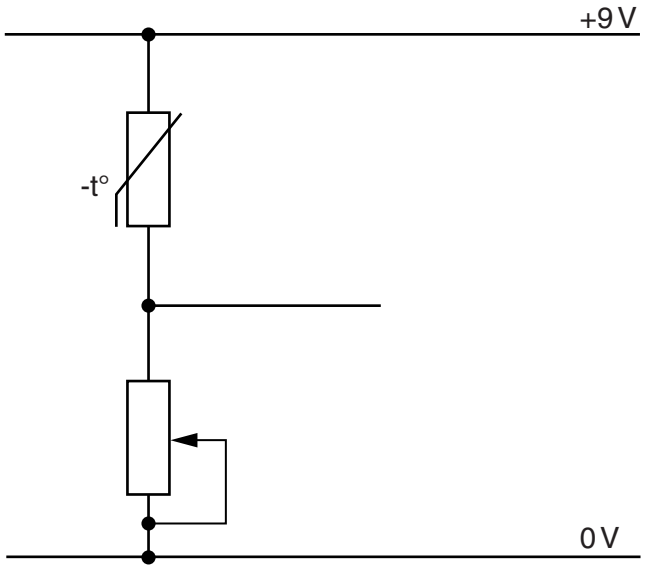
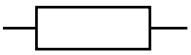
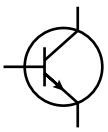
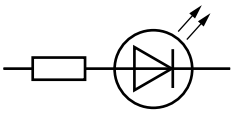


Fig. 5

(a) Label the diagram in Fig. 5 to identify the NTC thermistor. **[1]**

(b) Complete the circuit diagram in Fig. 5 by adding the symbols shown in the table below. **[3]**

Component	Symbol
base resistor	
npn transistor	
LED with a protective resistor	

(c) Label the transistor with the terms emitter(e), collector(c) and base(b). **[1]**

(d) Explain in detail how the circuit works.

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..... **[5]**

4 Fig. 6 shows a lighting circuit which has been short circuited (SC) between the live and neutral wires.

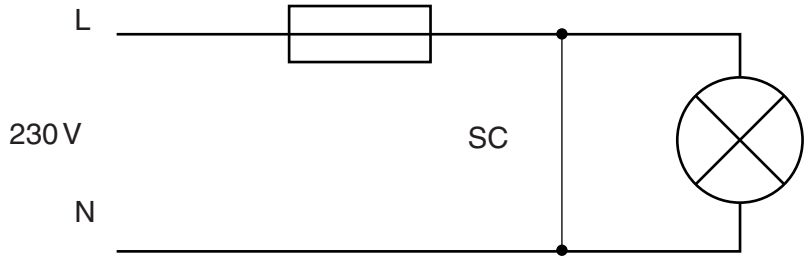

Fig. 6

(a) Explain why the circuit is not in a dangerous condition when the fuse blows.

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..... **[2]**

(b) Fig. 7 now shows the fuse in a different position and again short circuited.

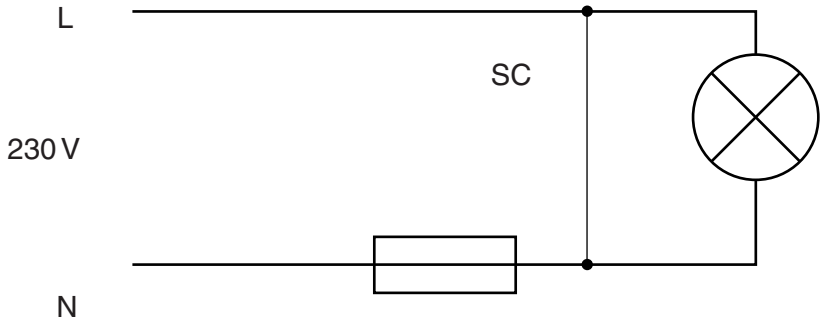

Fig. 7

Explain why the circuit is still dangerous even though the fuse has blown.

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..... **[3]**

(c) Fig. 8 shows a device that is used to prevent danger if there is a problem in an electrical circuit.

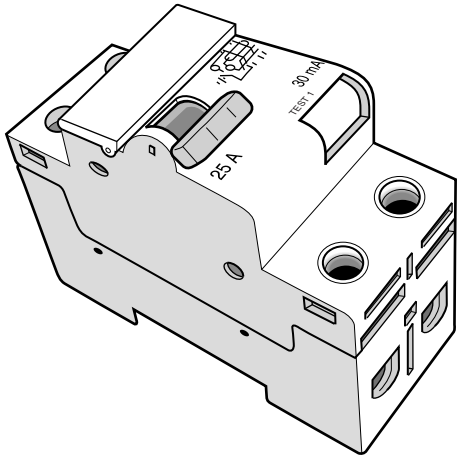

Fig. 8

(i) Name the device shown in Fig. 8.

..... **[1]**

(ii) Explain how the device works.

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..... **[4]**

5 **(a)** Complete the truth table shown below for a two-input AND, OR and NOR gate.

Input **A**	Input **B**	AND gate output	OR gate output	NOR gate output
0	0			
0	1			
1	0			
1	1			

[3]

(b) Explain what is meant by the terms logic level 1 and logic level 0 when used with logic gates.

logic level 1 .....

.....

logic level 0 .....

..... **[2]**

(c) Draw a diagram to show how a two-input NAND gate can be used as a NOT gate.

[2]

(d) State the main characteristics of an exclusive-OR gate (XOR).

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..... **[3]**

6 **(a)** Describe a quality assurance method used during commercial printed circuit board production including the finished product.

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..... **[4]**

(b)* Discuss the benefits and drawbacks to the manufacturer of using 'surface mount' technology compared to 'through hole' technology when manufacturing circuits.

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..... **[6]**

END OF QUESTION PAPER

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