

Cambridge National

Engineering

Unit **R113**: Electronic principles

Level 1/2 Cambridge National Award/Certificate in Systems Control in
Engineering

Mark Scheme for January 2016

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This mark scheme is published as an aid to teachers and students, to indicate the requirements of the examination. It shows the basis on which marks were awarded by examiners. It does not indicate the details of the discussions which took place at an examiners' meeting before marking commenced.

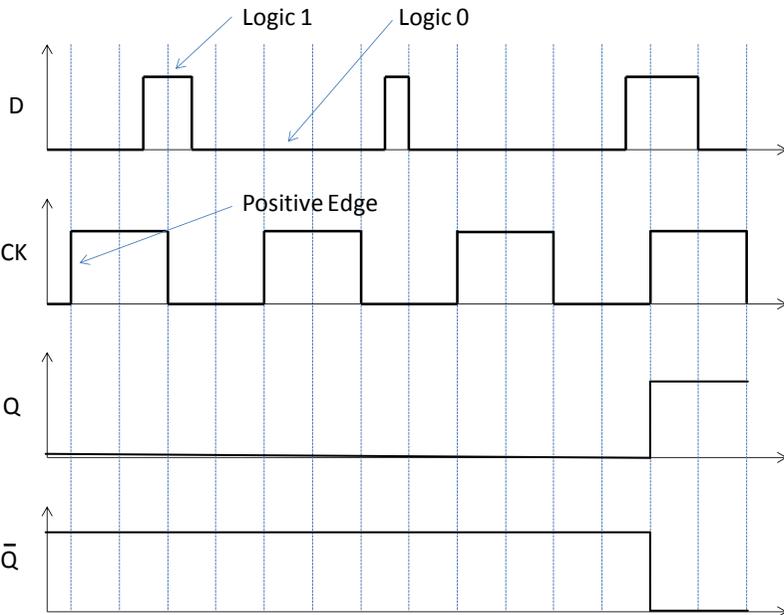
All examiners are instructed that alternative correct answers and unexpected approaches in candidates' scripts must be given marks that fairly reflect the relevant knowledge and skills demonstrated.

Mark schemes should be read in conjunction with the published question papers and the report on the examination.

OCR will not enter into any discussion or correspondence in connection with this mark scheme.

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Question			Answer	Mark	Guidance
1	(a)		Capacitance - farads Frequency - hertz	1 1	
1	(b)		The left hand diagram is a filament lamp and the right hand diagram is a signal lamp.	1 1	
1	(c)	(i)	$R = V/I$ $= 220/10$ $= 22\Omega$	1 1	Award one mark for a correct formula or 220/10. Award one mark for 22 or 22 Ω .
1	(c)	(ii)	$P = VI$ $= 220 \times 10$ $= 2200W$	1 1	Award one mark for a correct formula or 220 x 10. Award one mark for 2200 or 2200W or 2.2kW. Allow $P = V^2/R$.
1	(d)		Total resistance = 18 + 22 $= 40\Omega$	1 1	Award one mark for a correct formula or 18 + 22. Award one mark for 40 or 40 Ω .
Total				10	

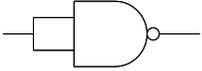
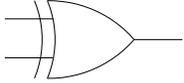
Question	Answer	Mark	Guidance
<p>2 (a)</p>	<p>Terminal D is the data input terminal and is where the flip-flop receives data. Terminal CK is the clock input. When a logic 1 is applied to the terminal, whatever signal is on the D terminal (0 or 1) is transferred to the Q terminal. Terminal Q is the output terminal. Terminal Q bar or NOT Q is another output terminal, which is the inverse of Q.</p>	<p>1 1 1 1</p>	<p>Accept: Terminal D – data input Terminal CK – clock input Terminal Q – output Terminal Q bar - output</p>
<p>2 (b)</p>	 <p>The diagram shows four vertically aligned waveforms over time. The top waveform is the data input D, with three pulses labeled 'Logic 1' and 'Logic 0'. The second waveform is the clock input CK, a square wave with four pulses labeled 'Positive Edge'. The third waveform is the output Q, which is low until the first positive edge of CK, then goes high. The bottom waveform is the inverted output Q-bar, which is high until the first positive edge of CK, then goes low. Vertical dashed lines connect the rising edges of CK to the corresponding logic levels of D and the state changes of Q and Q-bar.</p>	<p>1 1</p>	<p>Award one mark for correct answer only. Award one mark for correct answer only.</p>

Question	Answer	Mark	Guidance
<p>2 (c)</p>		<p>2</p> <p>2</p>	<p>Award one mark for correct positioning.↑</p> <p>Award one mark for correct shape.</p> <p>Award one mark for correct positioning.↑</p> <p>Award one mark for correct shape.</p>
Total		10	

		Answer	Mark	Guidance
3	(a)		1	Award one mark for NTC thermistor.
3	(b)		3	Award one mark for each of the following: npn transistor base resistor suitable output device.
3	(c)		1	Award one mark for correct labelling of b, c, and e.
3	(d)	<p>The thermistor and potentiometer act as a potential divider across the 9V supply. When the temperature of the thermistor rises, its resistance decreases. Current can now flow.</p> <p>The base resistor is designed to limit the current flow otherwise the transistor could be destroyed by overheating.</p> <p>This current goes through the base resistor into the base of the transistor, out of the emitter into the 0 volt supply line.</p> <p>The base current switches on the transistor collector current which activates the output device.</p> <p>The potentiometer can be adjusted to enable the output device to operate as required</p>	5	<p>Award up to five marks for a <u>description</u> that includes reference to:</p> <ul style="list-style-type: none"> • Potential divider • Thermistor • Base resistor • Transistor • Output device

Question			Answer	Mark	Guidance
4	(a)		The fuse is s correctly connected in the live line. When a fault occurs as a short circuit the fuse will blow and the lamp will be disconnected from the supply and be safe	1 1	
4	(b)		The fuse is incorrectly connected in the neutral line. When a fault occurs as a short circuit the fuse will blow. The lamp is not disconnected from the supply.	1 1 1	
4	(c)	(i)	Residual Current Device/RCD	1	
4	(c)	(ii)	Award marks for: When a fault is detected its purpose is to disconnect the mains supply. Works by detecting an imbalance of current flow from the live to neutral conductor. When a certain leakage current is detected, due to faulty equipment, or through someone touching the live conductor, then the RCD turns off the supply by tripping the switch. Leakage current is usually extremely small, usually below 30mA. The RCD is very fast acting.	1 1 1 1	

Question		Answer	Mark	Guidance																									
5	(a)	<table border="1"> <thead> <tr> <th>Input A</th> <th>Input B</th> <th>AND gate output</th> <th>OR gate output</th> <th>NOR gate output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input A	Input B	AND gate output	OR gate output	NOR gate output	0	0	0	0	1	0	1	0	1	0	1	0	0	1	0	1	1	1	1	0	3	Award one mark for each correct vertical column.
		Input A	Input B	AND gate output	OR gate output	NOR gate output																							
		0	0	0	0	1																							
		0	1	0	1	0																							
		1	0	0	1	0																							
1	1	1	1	0																									
5	(b)	<p>Logic level 1, known as high, is a voltage near the positive of the supply. Logic level 0, known as low, is a voltage near 0 volts.</p>	1 1	Accept ON and OFF as correct responses.																									

Question		Answer	Mark	Guidance															
5	(c)		1 1	<p>Award one mark for the NAND gate symbol.</p> <p>Award one mark for the single input.</p>															
5	(d)	 <p>The XOR gate is an OR gate with only two inputs, which gives a 'high' output when either input is high but not when both are high. Unlike the normal OR gate it excludes the case of both inputs being 'high' for a 'high' output.</p> <table border="1" data-bbox="349 735 1417 1251"> <thead> <tr> <th>Input A</th> <th>Input B</th> <th>Output Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input A	Input B	Output Q	0	0	0	0	1	1	1	0	1	1	1	0	1 1 1	<p>Award up to three marks for the explanation.</p> <p>The graphical symbol and the table are shown for reference.</p>
Input A	Input B	Output Q																	
0	0	0																	
0	1	1																	
1	0	1																	
1	1	0																	

Question		Answer	Mark	Guidance
6	(a)	<p>One method of QA is:</p> <p>Automatic Optical Inspection (AOI) of PCB assemblies using a Mirtec M3VL 5-camera 10 mega-pixel machine. This is a highly effective method for achieving non-contact quality assurance. It verifies component presence, orientation and value on dense SMT PCB assemblies. With full colour definition and complex software algorithms it also reliably checks solder joint quality using multiple camera angles. This process offers improvements in speed, coverage, cost and quality when compared with single camera AOI systems and conventional in-circuit test.</p> <p>AOI is not a full replacement for human inspection, which is carried out where appropriate using magnifying scopes etc for workmanship and build conformance</p>	4	<p>Award one mark for each correct point made up to a maximum of four.</p> <p>Award marks for any other correct method of carrying out Quality Assurance e.g. visual inspection.</p>

Question	Guidance	Mark	Answer
<p>6 (b)*</p>	<p>Level 3 (5–6 marks)</p> <ul style="list-style-type: none"> • Detailed discussion showing a thorough understanding of the benefits and drawbacks of SMT and THT. • Makes reasoned judgments about SMT and THT. • Information is presented clearly and accurately, with correct use of appropriate technical language and engineering terminology. • Accurate use of spelling, punctuation and grammar. <p>Level 2 (3–4 marks)</p> <ul style="list-style-type: none"> • Adequate discussion showing some understanding of the benefits and drawbacks of SMT and THT. • Makes some appropriate judgments about SMT and THT. • Information is presented clearly and with some accuracy. • Appropriate technical language and engineering terminology is used on some occasions. • Occasional errors in spelling, punctuation and grammar. <p>Level 1 (1–2 marks)</p> <ul style="list-style-type: none"> • Basic discussion showing limited understanding of the benefits and drawbacks of SMT and THT. 	<p>6</p>	<p>Benefits and drawbacks for the manufacturer of using SMT compared to THT.</p> <ol style="list-style-type: none"> 1 SMT has lower initial cost and time of setting up for production than THT. 2 SMT has a simpler and faster automated assembly system than THT. 1 SMT with smaller components has helped in solving the space problems that happened with the THT. 2 The pin count has increased in SMT when compared to THT 3 In SMT, the components do not have leads and are directly mounted to the board surface. 4 In THT the components have lead wires that are taken to the wiring boards via holes. 5 The pads on the surface in SMT are not used for connection of layers on the printed wiring boards. 6 THT components are larger which leads to lower component density per unit area. 7 The packing density that can be achieved with SMT is very high so component can be mounted on both sides. 8 SMT has made possible a greater range of applications than THT 9 SMT is suitable for high volume production which results in a

Question	Guidance	Mark	Answer
	<ul style="list-style-type: none"> • Information presented is basic and may be ambiguous or badly presented. • There will be little or no use of technical language and engineering terminology. • Errors of spelling, punctuation and grammar may be intrusive. <p>Level 0 (0 marks)</p> <ul style="list-style-type: none"> • A response that is irrelevant and/or not worthy of a mark. <p>Annotate with 'Seen' at end of response.</p>		<p>lower cost per unit as compared to THT.</p> <p>10 SMT make high performance circuits in a very small size as compared to THT.</p> <p>11 THT has a lower investment in machinery and production is higher as compared to SMT.</p> <p>12 Designing, production, skill and technology required in implementing SMT is very advanced when compared to THT.</p> <p>13 THT production in board assembly is still useful in testing and prototype applications that may need manual adjustments and replacements.</p> <p>14 Technically SMT has a lower resistance and inductance at the connection</p> <p>15 With SMT small errors in component placement are corrected automatically as the surface tension of molten solder pulls components into alignment with solder pads.</p> <p>16 SMT has better mechanical performance under shake and vibration conditions.</p> <p>17 Many SMT parts cost less than equivalent THT..</p> <p>18 With SMT manual prototype assembly or component-level repair is more difficult than THT.</p> <p>19-SMT cannot be used directly with breadboards</p> <p>20 SMT is unsuitable for large, high-power, or high-voltage parts.</p>

Question			Guidance	Mark	Answer
					<p>21 SMT is unsuitable as the sole attachment method for components that are subject to frequent mechanical stress.</p> <p>22 THT are best used for high-reliability products that require stronger connections between layers. because THT component leads run through the board, allowing the components to withstand more environmental stress.</p> <p>23 THT often used in military and aerospace products that may experience extreme accelerations, collisions, or high temperatures.</p>
			Total	10	

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