

Electronics

Advanced GCE A2 H465

Advanced Subsidiary GCE AS H065

Mark Schemes for the Units

June 2009

HX65/MS/R/09

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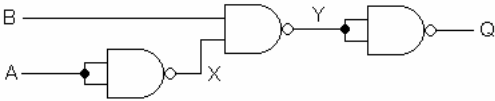
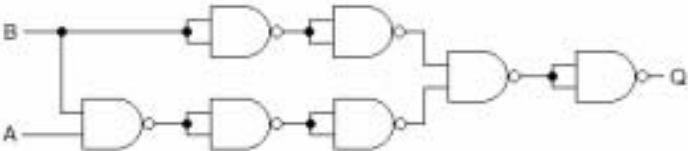
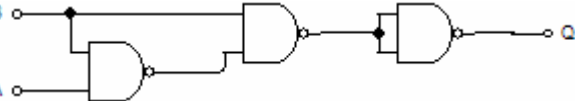
Advanced Subsidiary GCE Electronics (H065)

MARK SCHEMES FOR THE UNITS

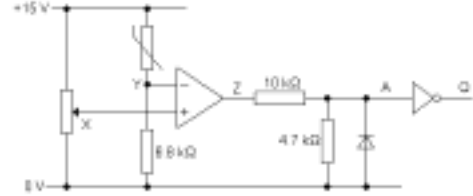
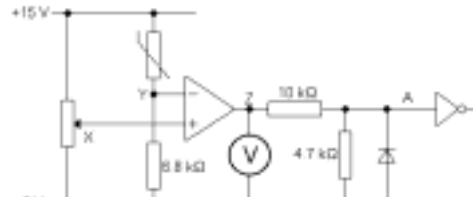
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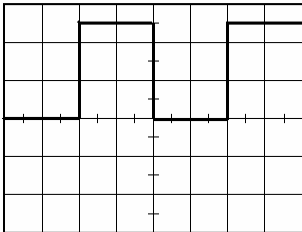
F611 Simple Systems

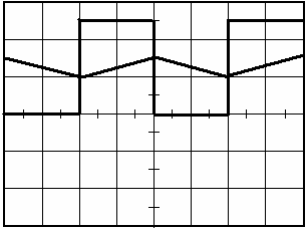
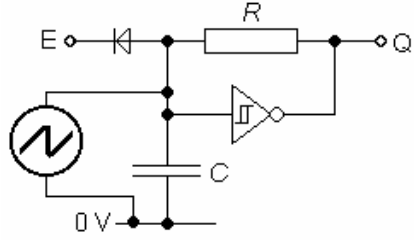
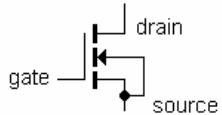
Question		Grade	Expected Answer	Mark	Additional Guidance																									
1	(a)	E E E	C = NOT B D = A AND B ecf: Q = C NOR D <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>B</th> <th>A</th> <th>C</th> <th>D</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	B	A	C	D	Q	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1	1	1	0	1	0	[3]	C column correct for [1] D column correct for [1] Q column correct for [1] If Q is incorrect, award [1] if Q is 1 only when both C and D are 0
B	A	C	D	Q																										
0	0	1	0	0																										
0	1	1	0	0																										
1	0	0	0	1																										
1	1	0	1	0																										
1	(b)	D	ecf incorrect Q: $Q = B.\bar{A}$ $Q = \overline{\bar{B} + A.B}$	[1]	expression which correctly matches table for [1]																									

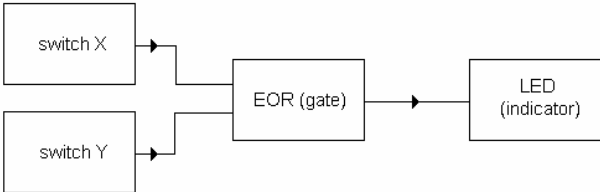
Question			Grade	Expected Answer	Mark	Additional Guidance
1	(c)		D C	<p>ecf incorrect Q: correct truth table [2] one error or omission [1] eg</p>  <p>OR</p>  <p>OR</p>  <p>No ecf from 1(b)</p>	[2]	<p>correct circuit, with or without X and Y, for [2] one mistake (missing A, B; incorrect symbol; missing gate...) for [1] circuit which matches incorrect truth table or expression for Q for [0]</p>

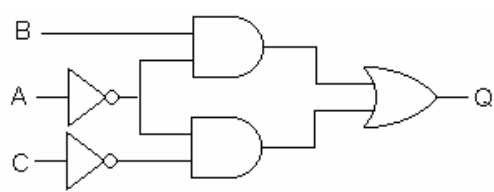
Question			Grade	Expected Answer	Mark	Additional Guidance																									
1	(d)		D E	EITHER correct use of Boolean algebra to link BA to Q $X = \bar{A}$, $Y = B.X$, $Q = \bar{Y}$ so $Q = B.X$, $Q = B.\bar{A}$ OR truth table with columns for all four input states and columns for outputs of all gates in the circuit eg <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>B</th> <th>A</th> <th>X</th> <th>Y</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	B	A	X	Y	Q	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	[2]	For Boolean algebra: correct expressions at outputs of each gate for [1] or correct expression for circuit in 1c for [1] correct combination of expressions to give Q [1] For truth table: columns for inputs and outputs of each gate for [1] all columns correct for [1] A truth table with any order of the four combinations of BA can earn [2]
B	A	X	Y	Q																											
0	0	1	1	0																											
0	1	0	1	0																											
1	0	1	0	1																											
1	1	0	1	0																											
2	(a)	(i)	E		[1]	any clear indication of thermistor for [1]																									
2	(a)	(ii)	D C	resistance depends on temperature (wtte) decreases with increasing temperature	[1] [1]	the resistance increases with increasing temperature for [1]																									

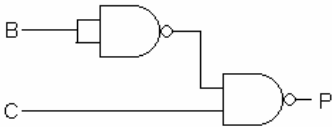
Question			Grade	Expected Answer	Mark	Additional Guidance
2	(b)	(i)	E	 <p>Correct symbol Correct connections to +15V, 0V and X</p>	[1] [1]	correct circuit symbol for [1] correct connections for [1] accept missing blobs
2	(b)	(ii)	D C B	Z starts at -13 V and ends at +13 V changing rapidly when X reaches same voltage as Y as non-inverting input rises above inverting input	[1] [1] [1]	May be implied from answer
2	(b)	(iii)	E		[1]	correct circuit symbol and connections for [1] accept missing blobs
2	(c)	(i)	D B	reverse biased very small current/very large resistance	[1] [1]	accept negative biased accept no current/ does not conduct
2	(c)	(ii)	E E C	$R = R_1 + R_2 = 14.7 \text{ k}\Omega$ ecf incorrect $R I = V/R = 13/14.7 \times 10^3 = 8.84 \times 10^{-4} \text{ A}$ ecf incorrect $I: V = IR = 8.84 \times 10^{-4} \text{ A} \times 4.7 \times 10^3 = 4.15 \text{ V}$	[1] [1] [1]	correct answer for [3] (accept 4.2 V) $I = 1.3 \times 10^{-3} \text{ A}$ or $2.8 \times 10^{-3} \text{ A}$ for [1] $V = 6.1 \text{ V}$ for [2]
2	(c)	(iii)	C B A	-0.7 V diode forward biased current rises rapidly with increasing voltage (owtte)	[1] [1] [1]	diode conducts at 0.7V when forward biased

Question			Grade	Expected Answer	Mark	Additional Guidance
2	(c)	(iv)	B A	logic 1 is above 3 V, logic 0 is anything below 2 V signals at A well away from the region of uncertainty	[1] [1]	Values close to 0V and 5V for [1]
3	(a)	(i)	C D E	$T = 0.5RC$ $R = 10 \text{ k}\Omega$ or more $T = 200 \times 10^{-6} \text{ s}$ (units conversion) ecf incorrect units conversion: $RC = 4.0 \times 10^{-4} \text{ s}$	[0] [1] [1] [1]	$R = 10 \text{ k}\Omega$ or more for [1] value of $R \times C = 4.0 \times 10^{-4} \text{ s}$ for [2] value of $R \times C = 4.0 \times 10^{-n}$ where $n \neq 4$ for [1] value of $R \times C = 2.0 \times 10^{-4} \text{ s}$ for [1] $R = 10 \text{ k}\Omega$ $C = 40 \text{ nF}$ [3]
3	(a)	(ii)	E D	$f = 1/T = 1/200 \times 10^{-6} = 5.0 \times 10^3 \text{ Hz}$ units conversion: 5 kHz	[1] [1]	5 kHz for [2] 0.05 kHz or 5000 kHz for [1]
3	(b)	(i)	E E D	correct shape (alternating high and low) one cycle in four divisions correct vertical displacements eg 	[1] [1] [1]	alternates between just two levels for [1] spends two squares at each level for [1] levels at centre and half a square from top for [1]

Question			Grade	Expected Answer	Mark	Additional Guidance
3	(b)	(ii)	C A B	correct shape (accept straight lines) correct phase correct maximum and minimum voltages 	[1] [1] [1]	rises gradually when output high, falls gradually when output low for [2] falls gradually when output high, rises gradually when output low for [1] goes between 1 square and 1.5 squares above centre for [1]
3	(b)	(iii)	E A	one connection to input with recognisable symbol or label "CRO" or "oscilloscope" another connection to 0 V 	[1] [1]	accept missing blobs
3	(c)	(i)	B	NOT gate output can't sink enough current	[1]	accept MOSFET increases current for the loudspeaker accept comments for power but not voltage
3	(c)	(ii)	C		[1]	accept g, d and s
3	(c)	(iii)	B A	drain-source resistance very large when gate below threshold voltage; falling to a very low value as gate goes above threshold voltage;	[1] [1]	Need to mention threshold (or V_{th}) for [2]

Question			Grade	Expected Answer	Mark	Additional Guidance																														
3	(d)		D C A	$I = V/R = 5/16 = 0.31 \text{ A}$ ecf incorrect $I: P = VI = 0.31 \times 5 = 1.56 \text{ W}$ average power is $1.56/2 = 0.78 \text{ W}$ (ecf)	[1] [1] [1]	0.78 W or 0.8 W for [3] 1.56 W or 1.6 W for [2] current = 0.3 A for [1] accept use of $P = V^2/R$																														
4	(a)	(i)	E E E		[3]	switch Y in input box for [1] Exclusive -OR/EOR (gate) in processor box for [1] accept logic gate as processor LED/light emitting diode in output box for [1]																														
4	(a)	(ii)	B	flow of information through the system	[1]	accept information or signals																														
4	(b)	(i)	E E E E	all combinations of switch settings closed switch gives a 1 (ecf) EOR truth table (ecf) LED only on when Q = 1 (ecf) <table border="1" data-bbox="555 794 1200 975"> <thead> <tr> <th>switch X</th> <th>switch Y</th> <th>B</th> <th>A</th> <th>Q</th> <th>LED</th> </tr> </thead> <tbody> <tr> <td>open</td> <td>open</td> <td>0</td> <td>0</td> <td>0</td> <td>off</td> </tr> <tr> <td>open</td> <td>closed</td> <td>0</td> <td>1</td> <td>1</td> <td>on</td> </tr> <tr> <td>closed</td> <td>open</td> <td>1</td> <td>0</td> <td>1</td> <td>on</td> </tr> <tr> <td>closed</td> <td>closed</td> <td>1</td> <td>1</td> <td>0</td> <td>off</td> </tr> </tbody> </table>	switch X	switch Y	B	A	Q	LED	open	open	0	0	0	off	open	closed	0	1	1	on	closed	open	1	0	1	on	closed	closed	1	1	0	off	[1] [1] [1] [1]	correct in all respects for [5]
switch X	switch Y	B	A	Q	LED																															
open	open	0	0	0	off																															
open	closed	0	1	1	on																															
closed	open	1	0	1	on																															
closed	closed	1	1	0	off																															
4	(b)	(ii)	E D	LED on when one switch pressed and only for this condition (owtte)	[1] [1]	LED on when only one switch pressed for [2] ecf from bi: all conditions for on [1] all conditions for on [1]																														
4	(c)	(i)	C D	limits the current/power of the LED so that it does not overheat	[1] [1]	Reduces voltage across LED damaged <u>by too much power/current</u> Not blown																														
4	(c)	(ii)	E	$I = P/V = 5 \times 10^{-3} / 1.7 = 2.9 \times 10^{-3} \text{ A}$	[1]	2.9 mA for [1]																														

Question			Grade	Expected Answer	Mark	Additional Guidance
4	(c)	(iii)	A E	$V = 5 - 1.7 = 3.3 \text{ V}$ ecf incorrect I or V : $R = V/I = 3.3/2.9 \times 10^{-3} = 1.1 \times 10^3 \Omega$	[1] [1]	1.1 k Ω or 1 k Ω for [2] 1.7 k Ω or 570 Ω for [1]
4	(d)		A	to improve clarity of circuit diagram (owtte)	[1]	
5	(a)	(i)	E E E	[1] for each correct term $\overline{C.B.A} + \overline{C.B.A} + C.B.A$	[3]	terms can be in any order must be these 3 terms, not backwards from ii
5	(a)	(ii)	A A A	insertion of brackets: $Q = (C + \overline{C}).B.\overline{A} + \overline{C.B.A}$ $C + \overline{C} = 1$ so $Q = B.\overline{A} + \overline{C.B.A}$ $Q = B.\overline{A} + \overline{C.B.A} + \overline{C.A}$ eliminate term to obtain $Q = B.\overline{A} + \overline{C.A}$	[1] [1] [1]	correct use of brackets and $C + \overline{C} = 1$ for [1] correct use of Race Hazard Theorem for [1] correct use of Redundancy Theorem for [1] Addition of any term (even incorrect) for [1] Use of any rule correctly [1] on each occasion
5	(a)	(iii)	E E E	final OR gate correct intermediate AND gates correct initial NOT gates 	[1] [1] [1]	

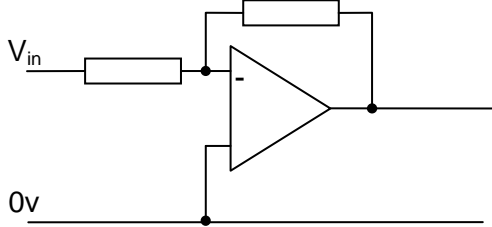
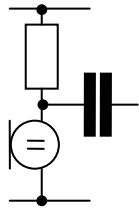
Question			Grade	Expected Answer	Mark	Additional Guidance
5	(b)	(i)	A B	accept circuit that works with more than 2 gates for [1] 	[2]	correct circuit for [2] one error or omission for [1] NAND symbol not correct (e.g NOR used) [1]
5	(b)	(ii)	A B	$P = \overline{\overline{B} \cdot C}$ $P = \overline{\overline{B}} + \overline{C} = B + \overline{C}$	[1] [1]	Correct expression for 5b(i) [1]
5	(b)	(iii)	E B	often need fewer integrated circuits making more of one i.c. makes it cheaper (owtte)	[1] [1]	
6	(a)		E E	$C = 33 \times 10^{-6} \text{ F}$, $R = 470 \times 10^3 \Omega$ (units conversion) ecf: $RC = 16 \text{ s}$	[1] [1]	15.5 s or 16 s for [2] $1.6 \times 10^n \text{ s}$ where $n \neq 1$ for [1]
6	(b)		A B C	capacitor immediately discharged through switch gate input goes low, output goes high <u>mosfet</u> switches lamp on	[1] [1] [1]	
6	(c)		D A B E	capacitor charges up (through resistor) taking $0.7RC = 11 \text{ s}$ before input goes high and output goes low turning <u>mosfet</u> and lamp off	[1] [1] [1] [1]	

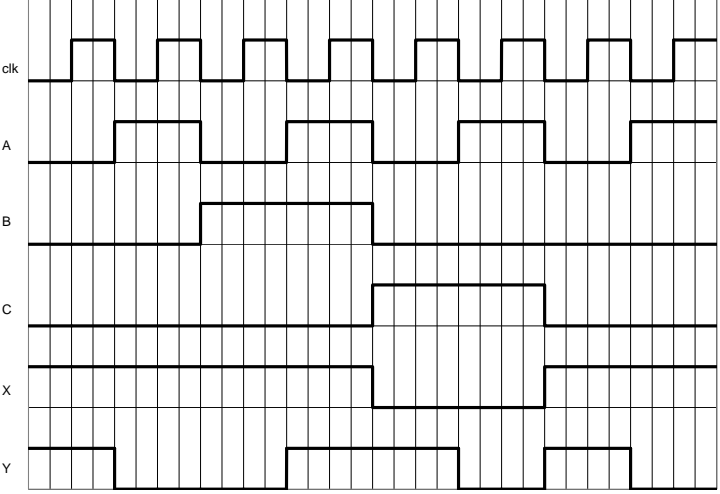
Quality of Written Communication

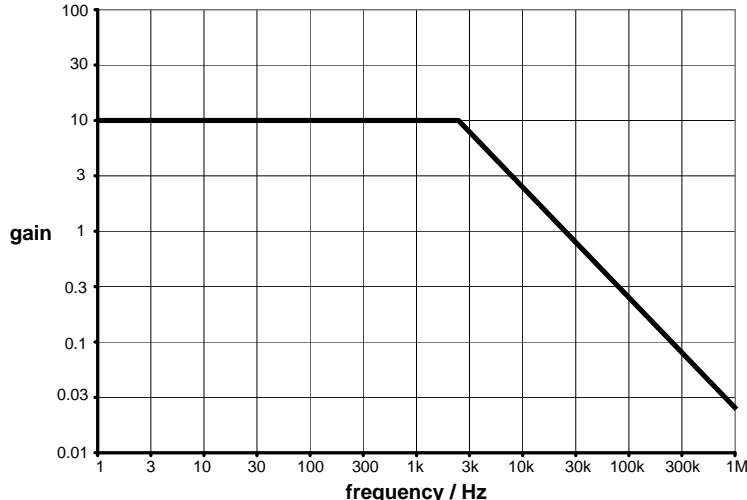
- 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
- 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
- 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
- 0 The language has no rewardable features.

F612 Signal Processors

Question		Syllabus Ref	Grade	Expected Answer	Mark	Rationale															
1	(a)		E	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>First three lines the same, last line different All correct</p>	A	B	Output	0	0	1	0	1	1	1	0	1	1	1	0	[1] [1]	
A	B	Output																			
0	0	1																			
0	1	1																			
1	0	1																			
1	1	0																			
1	(b)		E D C	Alarm turns on (owtte) Movement sensor produces a 0 at A When A is 0 then Q is 1 regardless of B (wtte) NO ecf from (a)	[1] [1] [1]	NOT goes off ACCEPT reference to NAND gate behaviour															
1	(c)		D C B A	D = 1 Alarm continues to sound (owtte) Q = 1 and D = 1 so B = 0 B = 0 (and A = 1) so Q = 1 NO ecf from (a)	[1] [1] [1] [1]	may be in third marking point															
2	(a)		E D	$G = \frac{V_{out}}{V_{in}} = \frac{1.2}{-0.2} = -6$ (even if sign missing) Minus sign	[1] [1]	ACCEPT 6 for [1] ecf incorrect value															

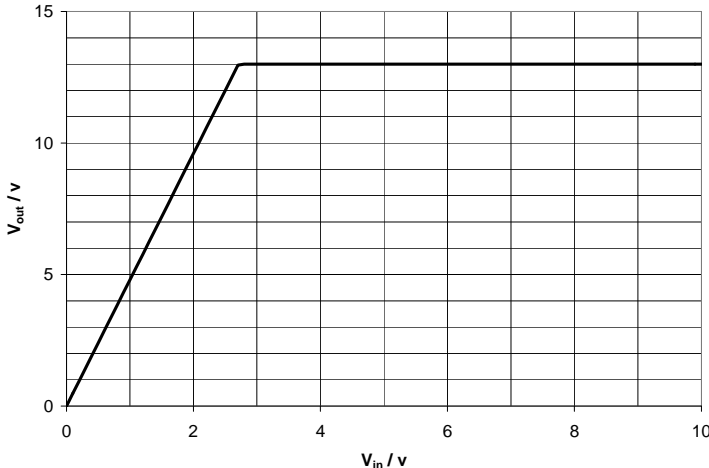
Question	Syllabus Ref	Grade	Expected Answer	Mark	Rationale
2 (b)		E E C B B	resistor provides negative feedback other resistor to input and non-inverting terminal to 0 V Labels indicating input and output Both resistors between 100 Ω and 10 MΩ $R_f:R_i = 6:1$ 	[1] [1] [1] [1] [1]	ACCEPT arrangement for non-inverting amplifier if gain in (a) is positive. ACCEPT ecf for gain in (a)
2 (c)		C E E	Pull-up resistor in series with microphone Capacitor from microphone to amplifier input Correct symbols (even if circuit wrong) 	[1] [1] [1]	ACCEPT microphone symbol without = IGNORE polarity of capacitor
3 (a) (i)		B E E D C	\bar{Q} to D on each flip-flop \bar{Q} to clock of next flip-flop clock input (ck) to clock of first flip-flop through NOT gate counter outputs from Q of flip-flops outputs labelled A, B and C from left to right	[1] [1] [1] [1] [1]	
3 (a) (ii)		B E	Connections from B and C to AND gate whose output goes to R on all flip-flops	[1] [1]	ecf from (i) ACCEPT R of first-flip-flop at 0 V all the time and AND gate to other two

Question			Syllabus Ref	Grade	Expected Answer	Mark	Rationale					
3	(b)	(i)		E A	Column X correct Column Y correct	C	B	A	X	Y	[1] [1]	
						0	0	0	1	1		
						0	0	1	1	0		
						0	1	0	1	0		
						0	1	1	1	1		
						1	0	0	0	1		
						1	0	1	0	0		
3	(b)	(ii)		E E E C D A	 <p>A correct all the way along B changes on first two falling edges of A C rises on first falling edge of B B and C reset on third falling edge of A X inverse of C Y high whenever A and B are the same</p>	[1] [1] [1] [1] [1] [1]	ALLOW ecf on A ALLOW ecf on B ALLOW ecf on A ALLOW ecf on C					

Question		Syllabus Ref	Grade	Expected Answer	Mark	Rationale
4	(a)		E	Treble cut filter	[1]	ACCEPT any unambiguous indication
4	(b)		D C B	Correct R identified (470 kΩ) $f = \frac{1}{2 \times \pi \times 470 \times 10^3 \times 150 \times 10^{-12}} \text{ (units conversion)}$ f=2260 Hz (ecf) ACCEPT 2200 Hz, 2300 Hz	[1] [1] [1]	NOT just correct formula ACCEPT 22.6 kHz for [2] if 47 kΩ used ACCEPT ecf on incorrect units conversion
4	(c)		E	$G = \frac{-R_f}{R_i} = \frac{-470 \times 10^3}{47 \times 10^3} = (-)10$	[1]	IGNORE sign of gain
4	(d)		E E B A	 <p>Correct shape (ecf from (a)) Flat at G = 10 (ecf from (c)) Breaks between 1 kHz and 3 kHz (ecf from (b)) Falls off at decade per decade (by eye)</p>	[1] [1] [1] [1]	ACCEPT some rounding at break point

Question		Syllabus Ref	Grade	Expected Answer	Mark	Rationale
5	(a)		E D	Any two valid points from: <ul style="list-style-type: none"> • Easier to design • Cheaper • Quicker to develop • Fewer parts / smaller circuit / less to wire up • Easier to make changes 	[1] [1]	
5	(b)	(i)	E	0100 1000 (one mark for each correct nibble)	[2]	
5		(ii)	D	48	[1]	ACCEPT ecf from (b)
5	(c)		E C D B B B A A	Output 00001000 to turn on beeper (and turn off LEDs) Wait for 0.5s / 500 ms Turn off beeper (and LEDs) b for Z switch, c for Y switch, d for X switch If no switch pressed go back to check switches again	[1] [1] [1] [1] [3] [1]	NOT just 08 Branch to b , c or d depending on state of switches for [1] Each branch corresponds to a different switch pressed for [2]

Question		Syllabus Ref	Grade	Expected Answer	Mark	Rationale
5	(d)		D A E C A	all boxes correct shape, syntax and arrows from b to a outputs byte X8 (in two steps) where X is 8, 4 or 2 pauses for 1000 (ms) outputs byte X0 (in two steps) X is 8 and X0 is loaded into A0	[1] [1] [1] [1] [1]	ecf incorrect syntax, shape ... ACCEPT last two processes in reverse order IGNORE \$, H ... in front of hex bytes IGNORE any extra steps which don't affect function of the routine If extra steps written, award marks for each required process completed
				<pre> graph TD b((b)) --> P1[let A0 = X8] P1 --> O1[/let output = A0/] O1 --> P2[pause 1000] P2 --> P3[let A0 = X0] P3 --> a((a)) </pre>		
6	(a)		E E	Show: $G = 1 + \frac{180 \times 10^3}{47 \times 10^3}$ $G = 4.8$	[1] [1]	ACCEPT 1 + 180/47 ACCEPT (-)3.8 for [1]
6	(b)		E E	Correct voltmeter symbol connected between V_{out} and 0 V	[1] [1]	look for a circle with V inside

Question	Syllabus Ref	Grade	Expected Answer	Mark	Rationale
6	(c)	E E	$V_{out} = G \times V_{in} = 0.6 \times 4.8$ (eor) $V_{out} = 2.9 \text{ V}$	[1] [1]	ACCEPT ecf from (a): 5 gives 3 V, 3.8 gives 2.3 V
6	(d)	E A C B	 <p>Straight line through origin of gradient 4.8 (by eye) e.g. goes through (1, 4.8) Saturates at 13 V</p>	[1] [1] [1] [1]	ACCEPT ecf from (a) or a gain of 5
7	(a)	E E D C	one second after shows 1 (on left or right) two to seven seconds after show 2, 3, 4, 5, 6, and 7 eight seconds after shows 0 nine and ten seconds after show 0	[1] [1] [1] [1]	
7	(b)	E E E C B	When switch pressed flip-flop set (owtte) When $Q = 1$, pulses pass through NAND gate to counter. Number at counter outputs goes up by one each second At 8 th pulse / when D goes high, counter and flip-flop reset Subsequent clock pulses blocked by NAND gate	[1] [1] [1] [1] [1]	ACCEPT Q goes high

Question		Syllabus Ref	Grade	Expected Answer	Mark	Rationale
8	(a)			Show: $5.6/5 = 1.12 \text{ V}$	[1]	
8	(b)			EITHER When switch released no current drawn through ($2 \text{ M}\Omega$) output impedance so no voltage drop inside the sensor OR When switch pressed, current is drawn through ($2 \text{ M}\Omega$) output impedance resulting in a voltage drop inside the sensor	[1] [1] [1]	ACCEPT responses in terms of voltage dividers instead of currents
8	(c)			EITHER $I = \frac{1.12}{1 \times 10^6} = 1.12 \times 10^{-6} \text{ A}$ 'lost' $V = 1.12 \times 10^{-6} \times 2 \times 10^6 = 2.24 \text{ v}$ $V = 1.12 + 2.24 = 3.36 \text{ v}$ OR 1.12 V across $1 \text{ M}\Omega$ so 2.24 V across $2 \text{ M}\Omega$ so sensor output = $2.24 + 1.12 = 3.36 \text{ V}$	[1] [1] [1]	ACCEPT correct use of voltage divider for [3] ACCEPT 3 V for [3]

Quality of Written Communication

- 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling.
- 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas.
- 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas.
- 0 The language has no rewardable features.

Grade Thresholds

Advanced GCE Electronics (H065 H465)
June 2009 Examination Series

Unit Threshold Marks

Unit		Maximum Mark	A	B	C	D	E	U
F611	Raw	90	59	52	45	39	33	0
	UMS	110	88	77	66	55	44	0
F612	Raw	90	56	49	42	36	30	0
	UMS	110	88	77	66	55	44	0
F613	Raw	80	63	55	47	39	31	0
	UMS	80	64	56	48	40	32	0

Specification Aggregation Results

Overall threshold marks in UMS (ie after conversion of raw marks to uniform marks)

	Maximum Mark	A	B	C	D	E	U
H065	300	240	210	180	150	120	0

The cumulative percentage of candidates awarded each grade was as follows:

	A	B	C	D	E	U	Total Number of Candidates
H065	27.4	39.4	56.0	69.1	81.7	100.0	487

497 candidates aggregated this series

For a description of how UMS marks are calculated see:
http://www.ocr.org.uk/learners/ums_results.html

Statistics are correct at the time of publication.

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