

# Unit 4: Principles of Electrical and Electronic Engineering

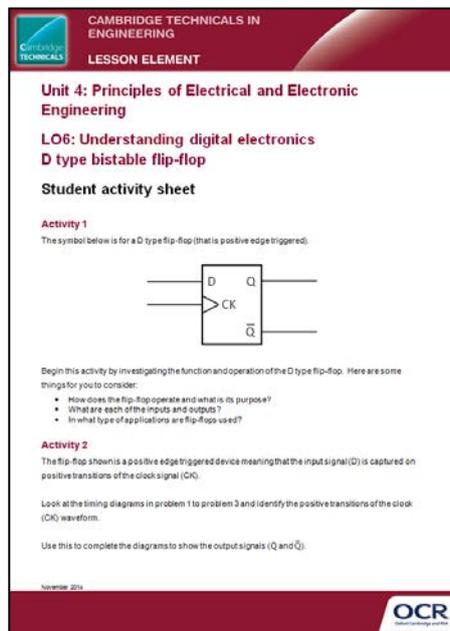
## LO1: Understand digital electronics

### D type bistable flip-flop

The expected duration is: 2 hours

### *Instructions and answers for teachers*

*These instructions should accompany the OCR resource ‘Understand digital electronics – D type bistable flip-flop’ activity which supports Cambridge Technicals in Engineering Level 3.*



The screenshot shows the OCR resource page for the D type bistable flip-flop activity. It includes the Cambridge Technicals logo, the unit title 'Unit 4: Principles of Electrical and Electronic Engineering', the learning objective 'LO6: Understanding digital electronics', and the specific topic 'D type bistable flip-flop'. The page is titled 'Student activity sheet' and contains two activities. Activity 1 asks students to identify the symbol for a D type flip-flop (positive edge triggered) and to investigate its function and operation. Activity 2 asks students to look at timing diagrams and identify the positive transitions of the clock (CK) waveform, and to complete the diagrams to show the output signals (Q and Q-bar). The OCR logo is visible in the bottom right corner of the page.

#### The Activity:

In this task the students investigate the functions and operations of a D Type flip-flop featuring a set of tasks.



*This activity offers an opportunity for English skills development.*



*This activity offers an opportunity for maths skills development.*

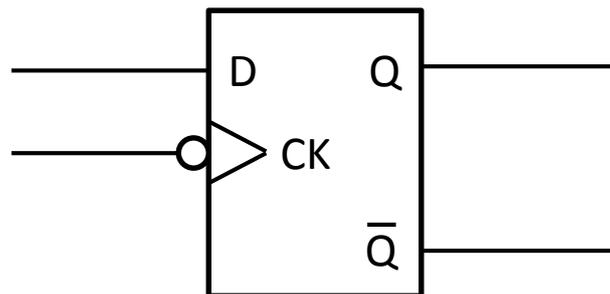
#### Suggested timings:

2 hours

### Activity 1

In Activity 1 learners are tasked to investigate the function and operation of the D type flip flop and to consider:

- How does the flip flop operate and what is its purpose?
- What are each of the inputs and outputs?
- In what type of applications are flip flops used?



### Solutions

- The D type flip flop is a latching device with outputs that have two stable states. This means that the output can be switched from logic 0 to logic 1, or logic 1 to logic 0 when required. Once set into either of these states it will remain there indefinitely so long as power is maintained to the device. For this reason it is often termed a 'bistable'.
- The purpose of a D type flip flop is to act as a latch or memory or storage device. It can store the information present on its inputs.
- The terminals are as follows:

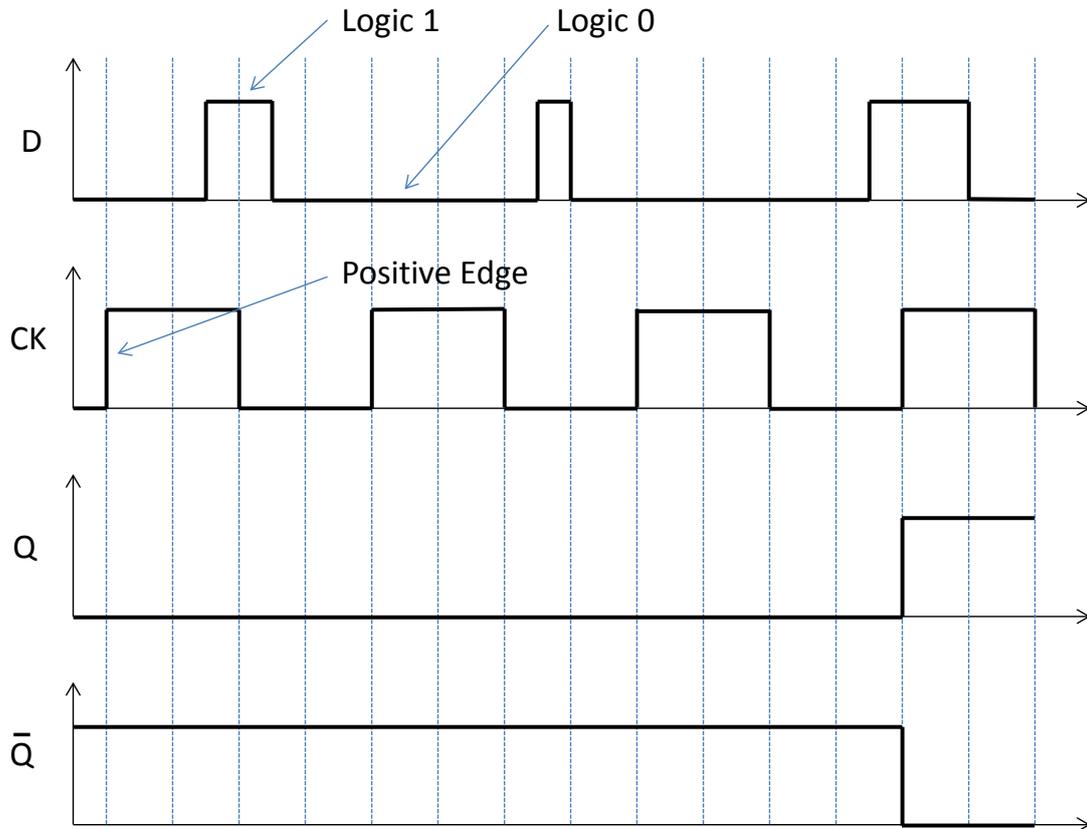
D	The terminal labelled D is called the data input terminal and is where the flip flop receives data
CK	CK is the clock input. When a logic 1 is applied to the terminal, whatever signal is on the D terminal (0 or 1) is transferred to the Q terminal. For the device shown this is usually referred to as rising edge triggered.
Q	Q is the output terminal
$\bar{Q}$	Q bar or NOT Q is another output terminal which is the inverse of Q

- Typical applications of the D type flip flop are: Latches, Counters, Memory Devices, Shift Registers.

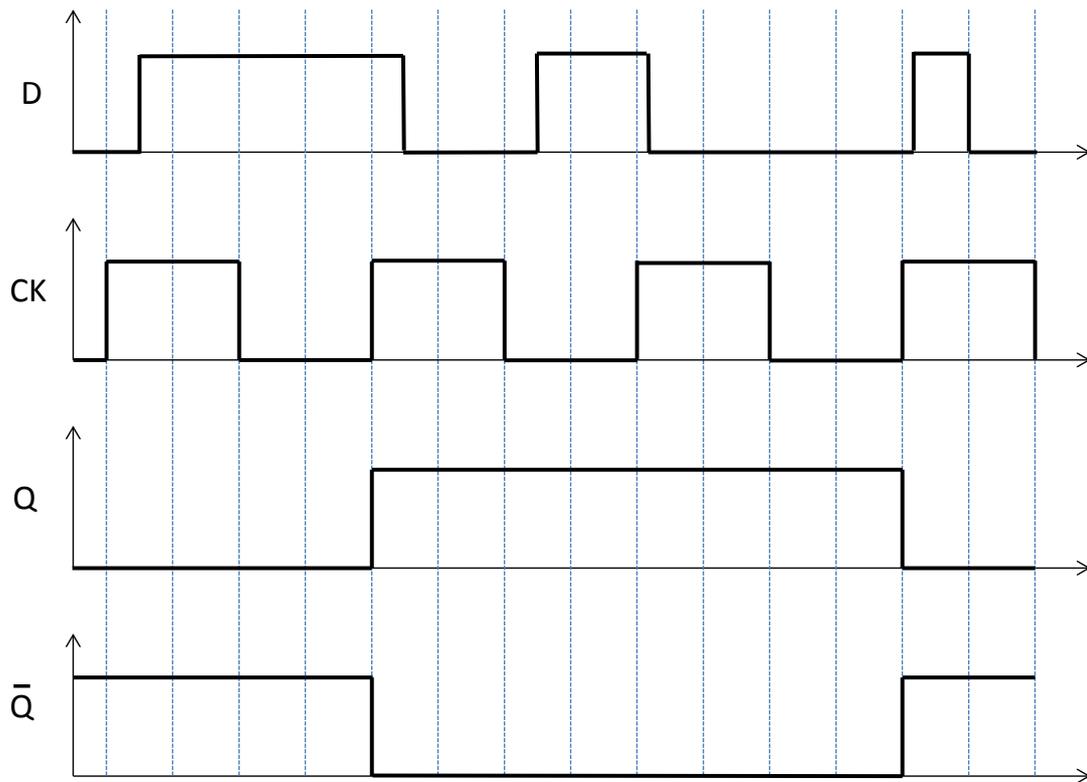
**Activity 2:**

In Activity 2 learners are asked to complete timing diagrams for a positive edge triggered D type flip flop. Solutions to Activity 2 are given below. Note that input signal D is captured on positive transitions of CK only. Learners are tasked to complete Q and  $\bar{Q}$ .

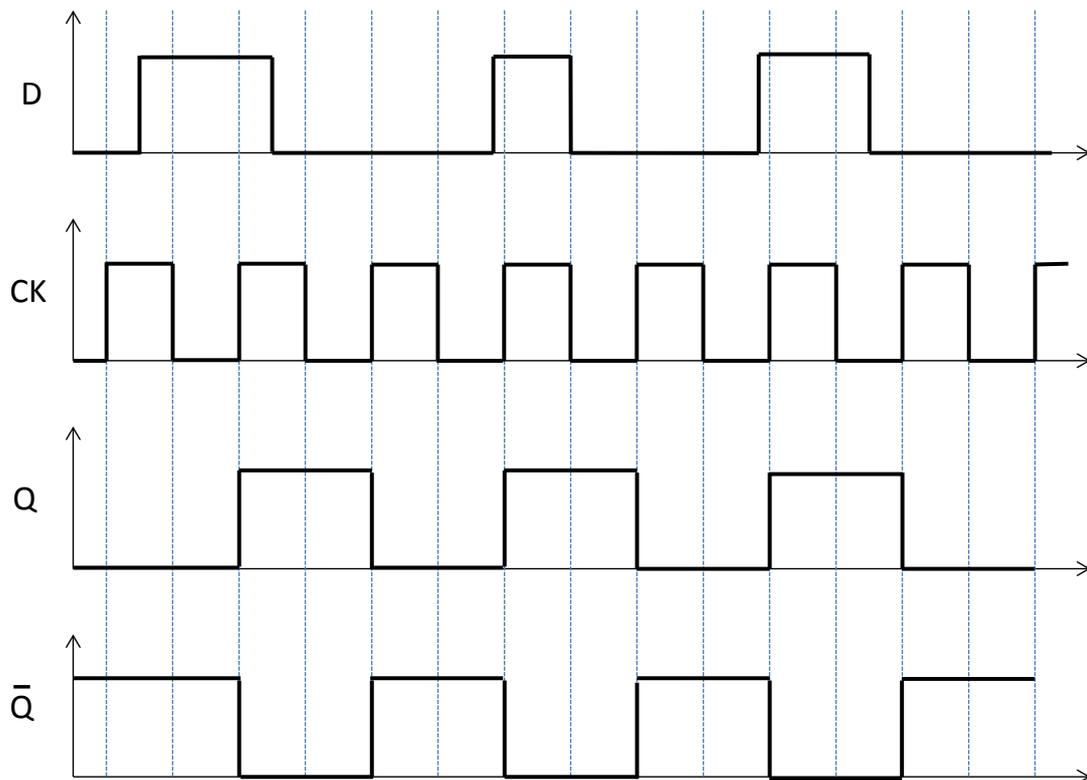
**Solution to Problem 1**



### Solution to Problem 2



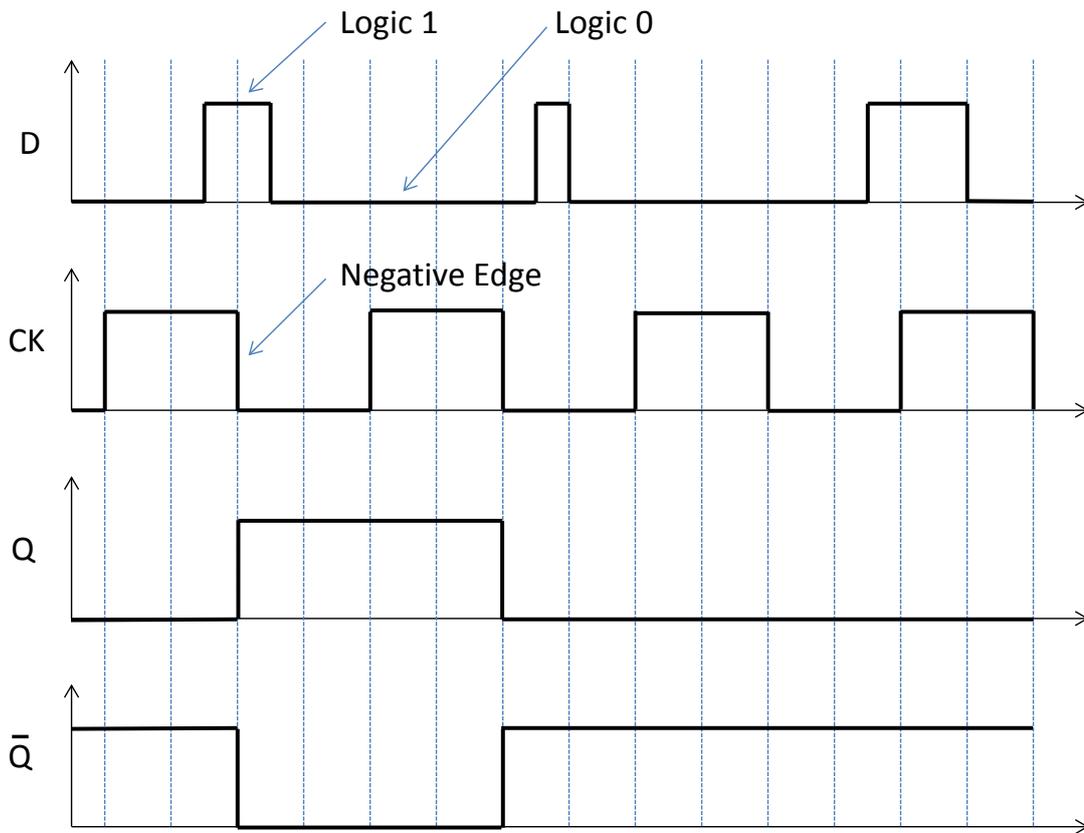
### Solution to Problem 3



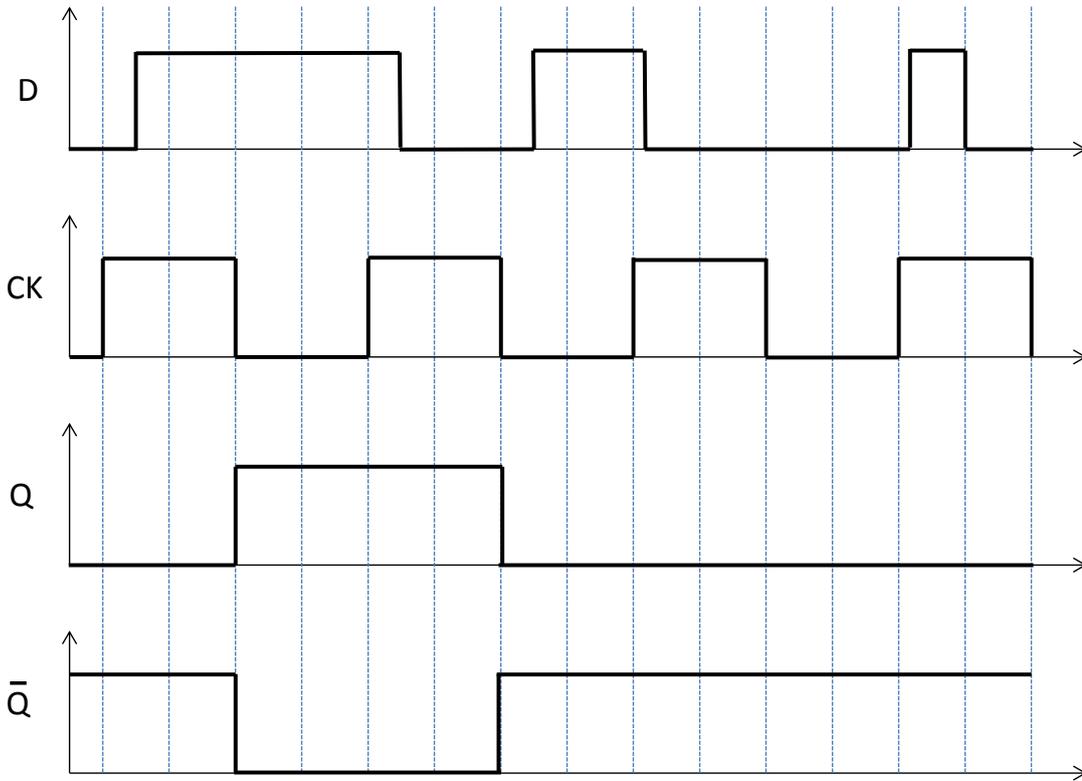
**Activity 3:**

In Activity 3 learners are asked to complete timing diagrams for a negative edge triggered D type flip flop. Solutions to Activity 3 are given below. Note that input signal D is captured on negative transitions of CK only. Learners are tasked to complete Q and  $\bar{Q}$ .

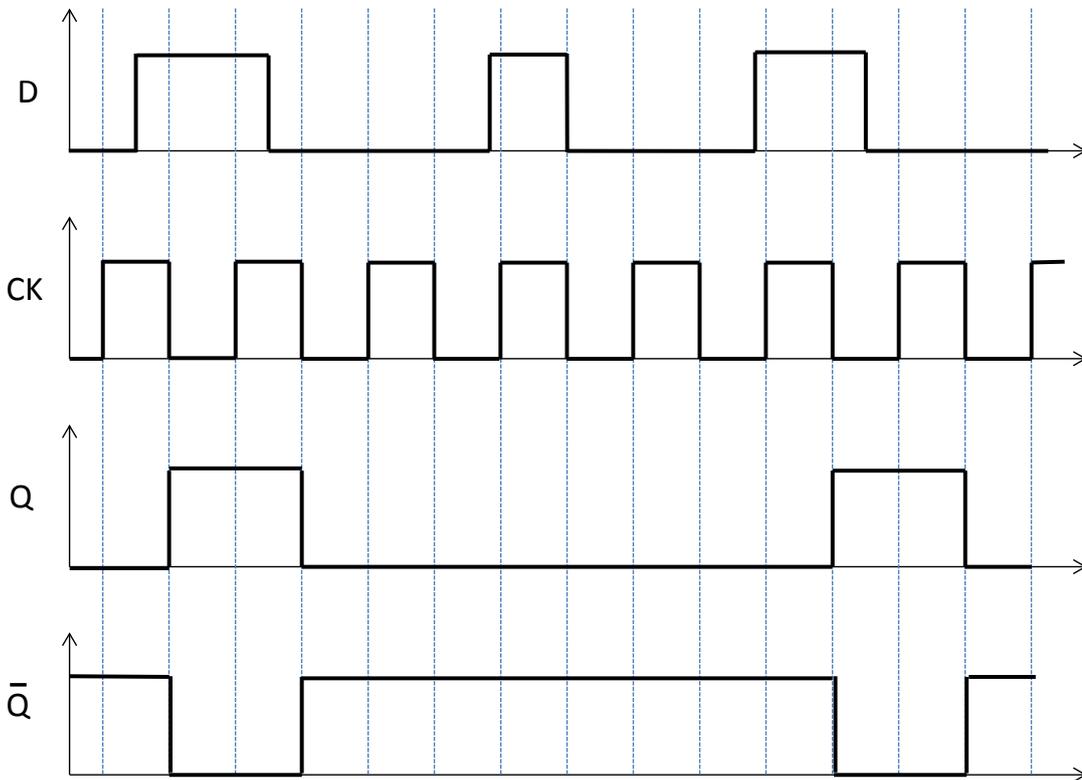
**Solution to Problem 4**



**Solution to Problem 5**



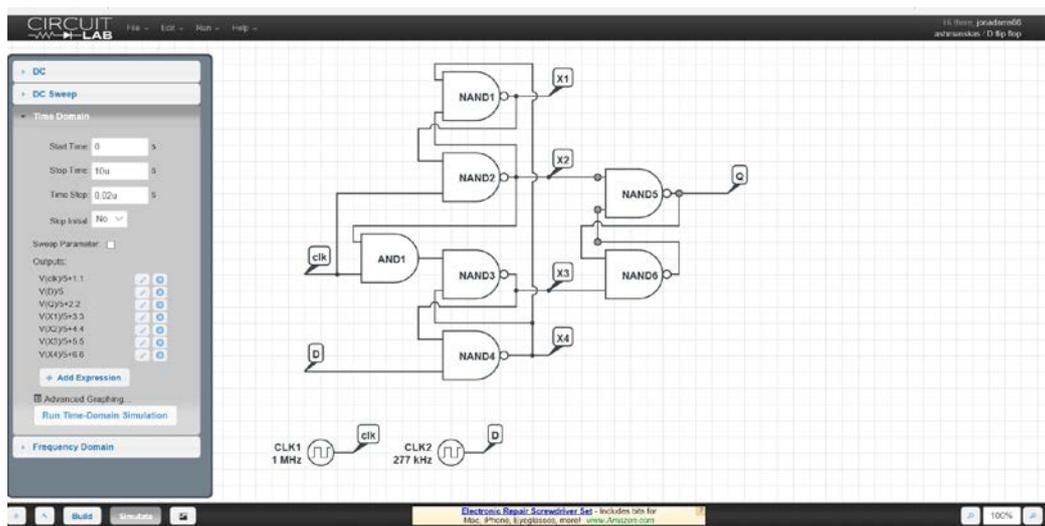
**Solution to Problem 6**



### Activity 4:

For Activity 4 learners are asked to consider building or simulating a circuit containing a D type flip flop. Learners may have access equipment where this could be undertaken practically. An alternative may be to undertake a simulation using simulation software. Learners have been provided with a link to a free web-based simulation tool. This tool is free and will simulate many different types of circuit. Free sign up is required.

<https://www.circuitlab.com/circuit/ywmw4t/d-flip-flop/>



The simulation provided produces a timing diagram from which learners might determine that the D type flip flop is operating correctly. Typical simulation results are shown below. These show a change in output with a change in input based on the clock transition (from high to low).



To complete the activity learners are tasked to explain the function of the S and R input pins on the D type flip flop. These are not shown in this simulation.

S	S is the SET input. Applying a logic 1 to the S input will make Q logic 1, and $\bar{Q}$ logic 0. This will happen irrespective of the state of any signal on the D or CK inputs
R	R is the RESET input. Applying a logic 1 to the S input will make Q logic 0, and $\bar{Q}$ logic 1. This will happen irrespective of the state of any signal on the D or CK inputs

It should be noted that S and R pins are present on most flip flop devices.



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